國立成功大學

111學年度碩士班招生考試試題

編　號：180、192、197

系　所：電機工程學系
電腦與通信工程研究所
電機資訊學院-微電、奈米聯招

科　目：電子學

日　期：0219

節　次：第 1 節

備　註：可使用計算機

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※ 考生請注意：本試題可使用計算機。　請於答案卷(卡)作答，於本試題紙上作答者，不予計分。

1. Fig. 1 shows an op amp connected in a closed loop with gain of +100 utilizing a feedback resistor of 1MΩ.
   (a) If the input bias current is 300 nA, what output voltage results with the input grounded ? (4%)
   (b) If the input offset is ±3 mV and the input bias current is 300 nA, what is the largest possible output voltage that can be observed with the input grounded ?. (4%)
   (c) If bias-current compensation is used, what is the value of the required resistor to be placed in series with the positive input lead ? If the offset current is no more than one-tenth the bias current (I_{OS}=30 nA), what is the resulting output offset voltage due to offset current alone ?(8%)
   (d) With bias-current compensation as in (c) in place, what is the largest dc voltage at the output due to the combined effect of offset voltage and offset current? (4%)

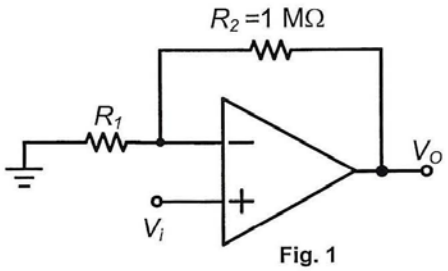

Fig. 1

2. The two-stage CMOS op amp in Fig. 2 is fabricated in a 0.18-μm technology with V_{tn} = -V_{tp} =0.6 V. If each of Q_1, Q_2, Q_3, and Q_4 is conducting a drain current of 100 μA and each of Q_6 and Q_7 is conducting a current of 200 μA. Assume that all transistors operate at 0.2-V overdrive voltages (V_{ov}=V_{GS}-V_{tn}=0.2 V).
   (a) Find the input common-mode voltage. (4%)
   (b) Find the allowable range of the output voltage. (4%)
   (c) With v_A=v_{id}/2 and v_B=- v_{id}/2, find the voltage gain v_o/v_{id}. Assume an Early voltage of 10 V. (4%)

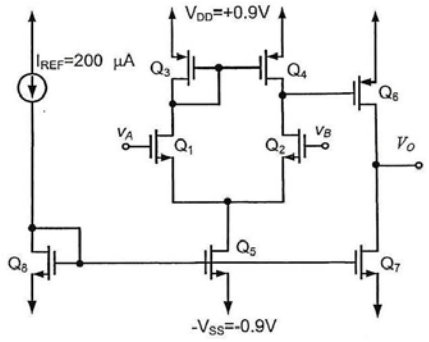

Fig. 2

3. Fig. 3 shows a shunt-shunt feedback amplifier. The MOSFETs have threshold voltage V_{tn}=0.6 V, Early voltage V_A=20 V, and $\mu_n C_{ox}$=200 μA/V². The power supply voltage V_{DD}=3.3 V, and R_L=2 kΩ. The coupling capacitor C_C can be assumed to be very large.
   (a) Perform a dc design to meet the following specifications: I_{D1}=100 μA, I_{D2}=1 mA, $I_{R2,R1}$=10 μA, overdrive voltage $V_{ov1,2}=V_{GS1,2}-V_{tn}$=0.2 V. Neglect the Early effect. Specify the values required for R_1 and R_2 (4%)
   (b) Find the value of R_S that results in V_O/V_S being ideally -6 V/V (2%)
   (c) Find the values of open-loop gain A, input resistance R_i, and output resistance R_o from open-loop circuit (6%)
   (d) Find the value obtained for V_O/V_S (2%)
   (e) Find R_{in} and R_{out} in Fig. 3 (4%)

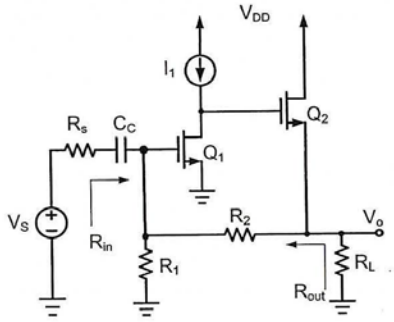

Fig. 3

4. Consider the circuit of Fig. 4. Given the op amps have saturation voltages of ±10 V and C=0.01 μF, R_1=20 kΩ, R_2=10 kΩ.
   (a) Sketch and label the waveforms (peak amplitude required) of v_{o1} and v_o. (8%)
   (b) Find the value of R_3 such that the resulted waveform frequency equals 1 kHz. (4%)

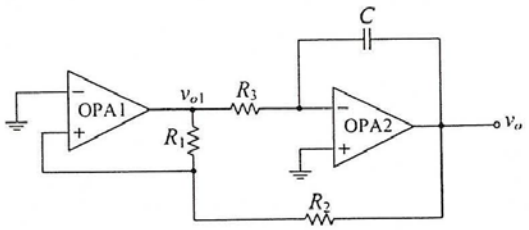

Fig. 4

5. The CMOS output stage of Fig. 5 is designed to operate at I_Q=1 mA with I_{BIAS}=0.1 mA. Assume that Q_1 and Q_2 are matched and Q_N and Q_P are matched, and each transistor operates at an overdrive voltage of 0.15 V in the quiescent state. Let $\mu_n C_{ox}$=250 μA/V², $\mu_p C_{ox}$=100 μA/V², V_{tn}=-V_{tp}=0.45 V, and V_{DD}=V_{SS}=2.5 V.
   (a) What kind of this output stage is (Hint: Class A, B, AB, C)? (3%)
   (b) Specify the (W/L) ratio for Q_1, Q_2, Q_N, and Q_P. (8%)
   (c) In the quiescent state with v_O= 0 V, what must v_I be? (4%)
   (d) If this output stage is required to supply a maximum load of 10 mA to R_L, find the maximum allowable output voltage (assume that I_{BIAS} needs a minimum of 0.2 V to operate properly). (5%)

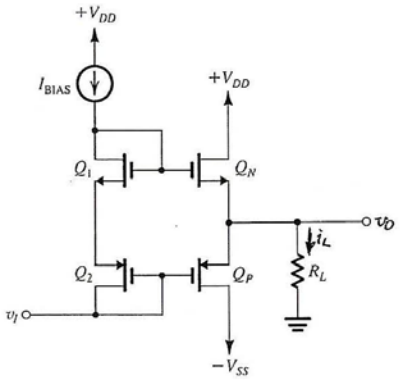

Fig. 5

6. For the filter circuit shown in Fig. 6, assuming the transconductance amplifiers are ideal.
   (a) Derive the transfer function: $\frac{V_o(s)}{V_i(s)}$ (3%)
   (b) Based on (a), find the values of G_{m1} and G_{m2} to achieve a low-pass filter with a pole frequency of 20 MHz and a DC gain of 10. Given C=2 pF. (6%)

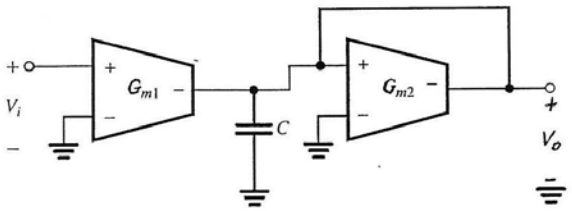

Fig. 6

7. For the 2nd order filter circuit shown in Fig. 7, assuming the op amps are ideal. Given $C_1=C_2=10$ nF, $R_3=14.14$ kΩ, and $R_4=7.07$ kΩ. Please find out the following filter's characteristics:
   (a) High-frequency gain (3%)
   (b) ω_0 (pole frequency, unit: rad/sec) (3%)
   (c) Q (pole quality factor) (3%)

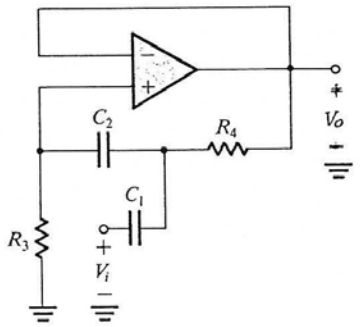

Fig. 7