國立成功大學
113學年度碩士班招生考試試題

編　號：194

系　所：電機資訊學院-微電、奈米聯招

科　目：固態電子元件

日　期：0201

節　次：第 2 節

備　註：可使用計算機

※ 考生請注意：本試題可使用計算機。　請於答案卷(卡)作答，於本試題紙上作答者，不予計分。

1. Assuming that the doping concentrations on the p-side and n-side of a pn junction are N_A and N_D, respectively, other required parameters should be set by yourself.
   (a) Derive the built-in voltage V_{bi} and the ratio of V_a/V_{bi}, where V_a is the voltage drop of the depletion region on the p side in thermal equilibrium. (10%)
   (b) Is there any current component in the depletion region of the pn junction in thermal equilibrium at room temperature? Why? (5%)
   (c) Plot the potential distributions of the pn junction in thermal equilibrium and under a forward bias V_F. Briefly explain the potential effect of V_F. (5%)
2. For a MOS(p) structure, if the flat-band voltage is zero.
   (a) Plot the high- and low-frequency C-V curves and explain why it is frequency-dependent. (5%)
   (b) Draw the V_s-V_G curve and briefly describe its physical significance, where V_G and V_s are the gate bias and the semiconductor voltage drop, respectively. (5%)
3. (a) Briefly explain why both BJT and MOSFET have switching electrical characteristics and can act as transfer resistors. (10%)
   (b) Briefly describe the physical concept of channel pinched-off in MOSFETs and the reason(s) for the saturation of drain current. (5%)
   (c) Draw the transfer characteristic (I-V) curve of an n-MOSFET in a semi-logarithmic plot, also indicate electrical parameters and operation regions on it. (5%)

The following are all single-choice questions

4. For semiconductor materials:

   (a) The mass action law, $np=n_i^2$ is **<u>NOT</u>** valid (5%)
   A. In the neutral regions of a forward-biased pn junction
   B. In a pn junction in thermal equilibrium
   C. Inside the source and drain regions of a MOSFET
   D. In a heavily-doped substrate of a CMOS wafer

   (b) Diffusion current is the dominating conduction mechanism for (5%)
   A. Minority carriers in a forward-biased pn junction
   B. Inversion carriers in a turned-on MOSFET
   C. Majority carriers in the source and drain regions of a MOSFET
   D. Conduction current in metal wires

(c) Which of the following statements about velocity saturation is **NOT** true? (5%)
   A. Saturation velocity is about 10^7cm/s for electrons; 8 x 10^6cm/s for holes
   B. Velocity saturation is due to optical phonon scattering when carrier momentum is very high
   C. The electron (hole) velocity is proportional to $\mu_n E$ ($\mu_p E$), where μ_n (μ_p) is the electron (hole) mobility and E is the horizontal (source-to-drain direction) electric field, no matter how large E is.
   D. In heavily velocity saturated MOSFET devices, the drain current is roughly proportional to $(v_{GS} - V_t)$, not $(v_{GS} - V_t)^2$

5. For n-channel MOSFETs:

(a) Body effect causes (5%)
   A. The threshold voltage of a MOSFET to increase
   B. The drain current of a MOSFET to increase
   C. The substrate doping concentration of a MOSFET to increase
   D. The gate insulator thickness of a MOSFET to increase

(b) Which of the following is **FALSE** about gate-induced drain leakage (GIDL) (5%)
   A. Occurs inside the drain region of a MOSFET
   B. Occurs when the gate voltage is very high and the MOSFET channel is inverted
   C. GIDL is significant when the drain voltage is high (near V_{dd})
   D. Is physically due to band-to-band tunneling

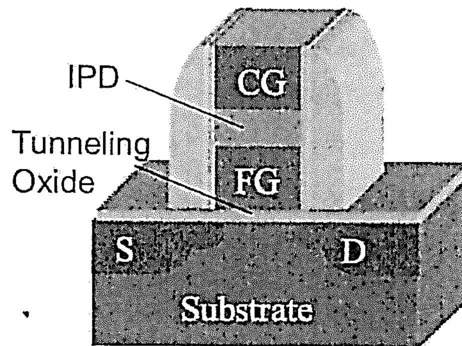
(c) Which of the following is **FALSE** regarding sub-threshold slope (swing) (5%)
   A. The theoretical minimum value for conventional MOSFET devices is 120mV/dec
   B. Is measured in the sub-threshold region when the MOSFET is not yet turned on
   C. Is improved (reduced) with forming gas annealing to reduce SiO_2/Si interface states
   D. Is improved (reduced) with the use of advanced device structures such as the FinFET

(d) Which of the following change to MOSFET structure increases its threshold voltage? (5%)
   A. Increase of (p-type) body doping
   B. Reduction of gate insulator thickness
   C. Use of gate material with lower work function
   D. Introduction of N-type dopants near the surface of the MOSFET

(e) Channel length modulation is due to which of the following when v_{DS} increases (5%)

A. Impact ionization near the drain end of the channel
B. Tunneling of electrons from gate to the drain region
C. Reduction of source-to-channel barrier height
D. Increment of drain-side depletion region width, causing reduction of effective channel length.

6. For the following floating-gate MOSFETs used in today's Flash memory, the inter-poly dielectric (IPD) has thickness t_{IPD}; the tunneling oxide has thickness t_{ox}; the width and length of the device is large-enough that parallel-plate capacitance formula applies, and there are negligible short-channel effects.



(a) The IPD capacitance per area is $C_{IPD} = \varepsilon_{IPD} / t_{IPD}$; the tunneling oxide capacitance per area is $C_{ox} = \varepsilon_{ox} / t_{ox}$, where ε_{IPD} and ε_{ox} are the dielectric constants of IPD/tunneling oxide. What is the voltage shift due to charge Q_{fg} in floating gate (FG). Threshold voltage is defined as the control gate (CG) voltage to turn on the floating-gate MOSFET. Q_{fg} may be positive or negative (5%)

A. $+ Q_{fg} / C_{ox}$
B. $+ Q_{fg} / C_{IPD}$
C. $- Q_{fg} / C_{ox}$
D. $- Q_{fg} / C_{IPD}$

(b) For Fowler-Nordheim (FN) tunneling to occur, so that electron tunnel from the channel (substrate) across the tunneling oxide into FG, but not into CG, upon application of positive voltage (+15V) on CG, what are the most plausible thicknesses of each of the layers (5%)?

A. $t_{IPD} = 4$nm; $t_{ox}=10$nm
B. $t_{IPD} = 10$nm; $t_{ox}=4$nm
C. $t_{IPD} = 20$nm; $t_{ox}=20$nm
D. $t_{IPD} = 2$nm; $t_{ox}=2$nm