國立成功大學
114學年度碩士班招生考試試題

編　號：146

系　所：電機資訊學院-微電、奈米聯招

科　目：半導體元件物理

日　期：0210

節　次：第 2 節

注　意：1.可使用計算機
　　　　2.請於答案卷(卡)作答，於試題上作答，不予計分。

1. For an NPN bipolar junction transistors, how do we increase (enhance) the current gain (β) (5%, single choice)?
   A. Increase the emitter doping
   B. Increase the base width
   C. Increase the base doping
   D. Increase the hole mobility/hole diffusion coefficient

2. In a planar bulk MOSFET, gate-induced drain leakage current flows from (5%, single choice)
   A. Drain terminal to source terminal
   B. Drain terminal to gate terminal
   C. Drain terminal to substrate terminal
   D. Gate terminal to substrate terminal

3. For MOSFETs, which of the following physical phenomenon does <u>NOT</u> affect the output conductance (g_{ds}) or output resistance (r_o) during on-state (5%, single choice)?
   A. Channel length modulation
   B. Drain-induced barrier lowering
   C. Gate-induced drain leakage
   D. Self heating effect

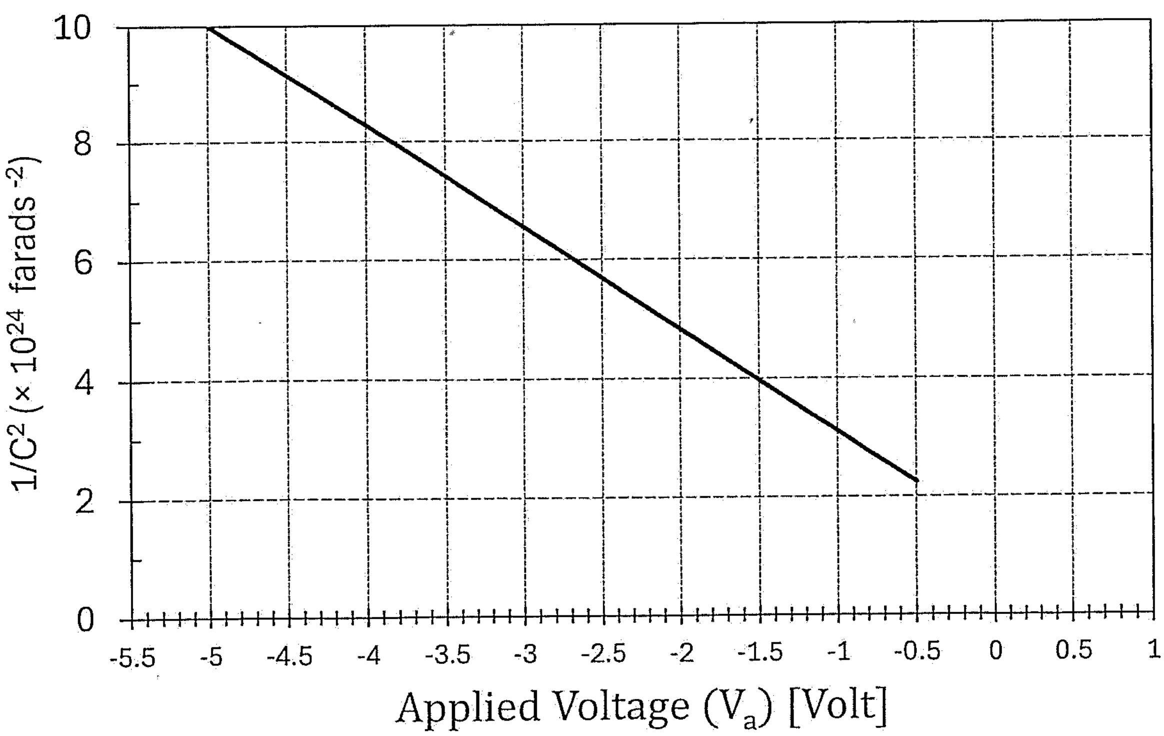
4. Which of the following is <u>NOT</u> true regarding velocity saturation in MOSFETs (5%, single choice)
   A. Causes the channel electron/hole velocity to reduce
   B. Causes drain current to reduce
   C. Happens when the channel length is very long
   D. Physically velocity saturation is due to optical phonon scattering

5. In MOSFETs, the inversion layer is not exactly at the silicon/SiO_2 interface (surface), but about 1.5 nm below. This is because (5%, single choice)
   A. Bad interface quality at MOSFET surface
   B. Quantum confinement causes electron/hole density to peak at 1.5nm below the surface
   C. Surface scattering effects
   D. The first few layers of the channel is not silicon

6. For a CMOS technology, how do we incorporate both n-MOSFETs and p-MOSFETs on the same substrate on a p-type silicon wafer (5%, single choice)?
   A. Place n-MOSFET in n-well and p-MOSFET in a p-well
   B. Place n-MOSFET in n-well and p-MOSFET directly in the p-type substrate
   C. Place n-MOSFET in p-well and p-MOSFET directly in the p-type substrate
   D. Place n-MOSFET directly in the p-type substate and p-MOSFET in an n-well

7. For a long channel n-MOSFET, the gate work function is 4.6eV; the channel material is silicon with a relative dielectric constant of 11.7; the channel is uniformly doped with boron at $10^{17}cm^{-3}$; the gate dielectric is HfO_2 with a dielectric constant of 23.4 and a thickness of 2.4nm, plus a SiO_2 interfacial layer with thickness of 0.6nm; the surface potential at threshold is 0.85V. The threshold voltage is V_{t0}=0.4V. (20%)
   1) Calculate the equivalent oxide thickness (EOT) without considering the effects of inversion layer thickness (5%).
   2) Assuming the inversion layer is on average 1.5nm below Si/SiO_2 interface in silicon, contributing to an additional 0.5nm in the EOT, calculate the oxide capacitance C_{ox} (per unit area) (5%)
   3) If we increase the gate work function to 4.8eV, calculate the change in threshold voltage $\Delta Vt = V_{t(new)}-V_{t0}$. (5%)
   4) If we increase the doping to 2 x 10^{17} cm^{-3} while keeping the gate work function at 4.6eV, calculate ΔV_t. (5%)

8. The figure below shows the room-temperature (300 K) capacitance–voltage (C–V) characteristics of a uniformly doped silicon PN junction diode. The graph is drawn to scale. Assume each side of the junction contains only one type of dopant (i.e., p-side is acceptor-only and n-side is donor-only). The doping concentration on the p-side (N_A) is 10 times higher than that on the n-side (N_D). All dopants are 100% ionized, and the diode's junction area is 2.1×10^{-5} cm^2. (13%)



The following physical constants might be needed in this question:

Free-space permittivity = $8.85\times10^{-14}\,F/cm$

Electronic charge = $1.6\times10^{-19}C$

Dielectric constant of Si = 11.9

Free electron mass $m_0 = 9.1 \times 10^{-31} kg$

Effective electron mass = $1.12\ m_0$; Effective hole mass = $0.8\ m_0$

Boltzmann constant $k = 1.38 \times 10^{-23} J/K$

Planck constant $h = 6.626 \times 10^{-34}$ J-s.

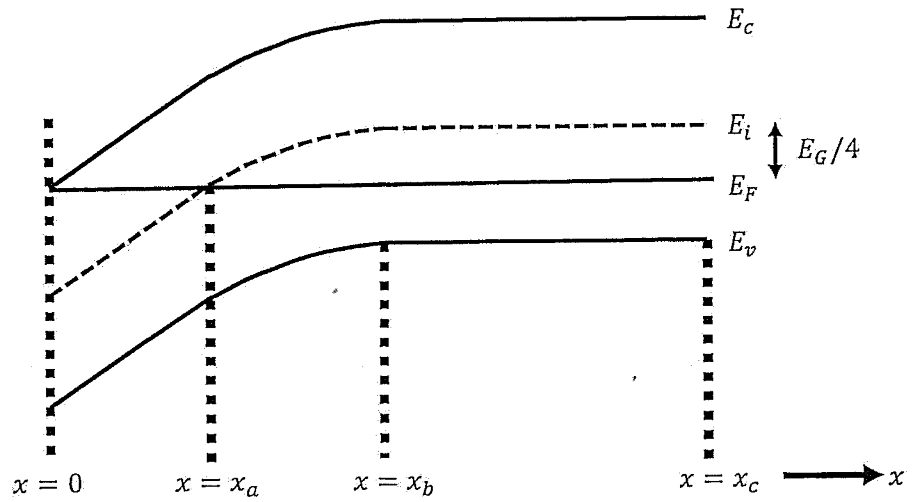
Answer the following questions:

(a) Find the built-in voltage (V_{bi}) of the junction in the units of volt. (3%)

(b) Calculate the dopant concentration on the lowly doped side of the diode in the units of cm^{-3}. (5%)

(c) Calculate the depletion width of the diode at $V_a = -1.5V$ in microns. (5%)

9. A semiconductor is characterized by the energy band diagram below. It is also known that $E_G = 1.12$ eV, $kT = 0.0259$ eV, $n_i = 10^{10}$ cm^{-3}, $\mu_n = 1350$ cm^2/Vs, $\mu_p = 460$ cm^2/Vs and $\tau_n = 10^{-4}$ s. (37%)



(a) Sketch the electrostatic potential and the electric field inside the semiconductor as a function of x, labeling the positions x = 0, x_a, x_b, and x_c. (6%)

(b) Sketch the **electron** concentration n as a function of the position x, indicate n_i. (4%)

(c) Calculate n at $x = x_a$ and $x = x_c$. (6%)

(d) Calculate the resistivity of the semiconductor at $x = x_a$ and $x = x_c$. (6%)

(e) Is there an electron drift current at $x = x_a$? Is there an electron diffusion current at $x = x_a$? What is the total electron current density J_n at $x = x_a$? Explain your answers but don't calculate numerical values for the diffusion and drift current. (6%)

(f) An electron at $x = x_b$ with total energy $E = E_C$ moves from $x = x_b$ to $x = 0$ without changing its total energy. What is the kinetic energy of the electron upon arriving at $x = 0$? (4%)

(g) By illumination, an excess of electron-hole pairs is generated at $x = x_c$ at a rate $G_L = 10^{19}$ cm^{-3} s^{-1}. Calculate the resistivity of the semiconductor at $x = x_c$ after illumination. (5%)