系所組別： 電腦與通信工程研究所甲組

考試科目： 計算機組織與作業系統　　　　　　　　　　考試日期：0220，節次：1

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請務必按照題號順序作答(否則不計分)，總分為 100 分。

1. What decimal number is represented by the biased single precision IEEE 754 floating point format? (10%)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	0	0	0	0	0	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

2. (a) Consider a five-stage pipelined processor that executes the MIPS code with an instruction and a data memory. Assume there is no forwarding in this pipelined processor. Indicate hazards and add "nop" instructions to eliminate them. (10%)

Instruction Sequence
lw $1,40($6)
add $6,$2,$2
sw $6,50($1)

(b) Assume that all branches are perfectly predicted. If we only have one memory (for both instructions and data), draw the pipeline stage and count the total execution clock cycles of the below instruction sequence in the five-stage pipeline that only has one memory? (10%)

Instruction Sequence
lw $5,-16($5)
sw $4,-16($4)
lw $3,-20($4)
beq $2,$0,Lbl ; Not taken
add $5,$1,$4

3. The parameters v[] and k are in argument register $a0 and $a1, respectively. Write the MIPS assembly codes for the following procedure. Use $t0, $t1 and $t3 in your codes. (10%)

```
void swap( int v[] , int k ) {
    int temp;
    temp = v[k];
    v[k] = v[k+1];
    v[k+1] = temp;
}
```

4. Assume 1 memory bus clock cycle to send the address, 15 memory bus clock cycles for each DRAM access initiated, 1 memory bus clock cycle to send a word of data. If we have a cache block of four words and a one-word-wide bank of DRAMs, what is the miss penalty? (10%)

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5. 20%
(a) What is the demand paging technique used in virtual memory systems.
(b) What is lazy swapper and how to transfer of a page between main memory and contiguous disk space in a demand-paging system.
(c) Please describe how to use hardware support to distinguish between the pages that are in memory and the pages that are on the disk.
(d) Please describe the six steps in handling a page fault.

6. 10%
(a) What is CPU scheduler.
(b) The Linux scheduler is a preemptive, priority-based algorithm with two separate priority ranges. Please describe how the Linux kernel maintains a list of all runnable tasks in a run queue data structures.

7. 10%
(a) What is a process.
(b) Please draw the state diagram of the corresponding states of a process.
(c) Please write down 5 pieces of information in a process control block associated with a specific process.

8. 10%
(a) Please describe the four necessary conditions of a deadlock situation.
(b) Please describe the methods for handling deadlocks.

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