1. Design a memory hierarchy system for a conventional five-stage pipeline processor. Assume both the virtual address and physical address are 32 bits. The page size is 32KB. ITLB has 48 entries and 3-way set associative. DTLB is direct-mapped, 32 entries. The data cache is physically addressed; cache size 32KB, direct-mapped, line size 64 bytes.

   a. Show a typical five stage pipeline diagram and explain their functionality. (10%)
   b. Show how to integrate the two TLBs to the pipeline. (10%)
   c. Explain the translation of virtual address to the physical address for ITLB. (10%)
   d. Design the data cache and integrate it with the DTLB by showing how the address lines are used. (10%)

2. Write down two possible causes for getting an illegal instruction. (10%)

3. What are the benefits and the disadvantages of each of the following? Consider both the system level and the programmer level.
   a. Synchronous and asynchronous communication. (4%)
   b. Automatic and explicit buffering. (4%)
   c. Send by copy and send by reference. (4%)
   d. Fixed-sized and variable-sized messages. (4%)

4. Explain why spinlocks are not appropriate for single-processor systems yet are often used in multiprocessor systems. (4%)

5. a. What is swapping. (5%)
   b. What is the context switch time, associated with swapping, if a disk drive with a transfer rate of 2 MB/s is used to swap out part of a program that is 200 KB in size? Assume that no seeks are necessary and that the average latency is 15 ms. The time should reflect only the amount of time necessary to swap out the process. (5%)

(背面仍有題目,請繼續作答)

6. Assume a program has just referenced an address in virtual memory. Describe a scenario how each of the following can occur: (If a scenario cannot occur, explain why.) (10%)
   a. TLB miss with no page fault.
   b. TLB miss and page fault.
   c. TLB hit and no page fault.
   d. TLB hit and page fault.

7. Why is it important for the scheduler to distinguish I/O-bound programs from CPU-bound programs? (5%)

8. Compare the circular-wait scheme with the deadlock-avoidance schemes (like the banker's algorithm) with respect to the following issues:
   a. Runtime overheads
   b. System throughput (5%)