

系所組別：電機工程學系甲乙丁戊組、電腦與通信工程研究所丙丁組、電機資訊學院-微電奈米聯招

考試科目：電子學

考試日期：0222，節次：1

※ 考生請注意：本試題可使用計算機。請於答案卷(卡)作答，於本試題紙上作答者，不予計分。

1. Fig. 1 shows a circuit that performs the high-pass transfer function.
  - (1) Derive the transfer function of this circuit and identify its high-frequency gain and 3-dB frequency. (4%)
  - (2) Determine the values of  $R_1$ ,  $R_2$ , and  $C$  to obtain a high-frequency input resistance of  $10\text{ k}\Omega$ , a high-frequency gain of  $40\text{ dB}$ , and a 3-dB frequency of  $1000\text{ Hz}$ . (6%)
  - (3) At what frequency does the magnitude of the transfer function reduce to unity? (4%)

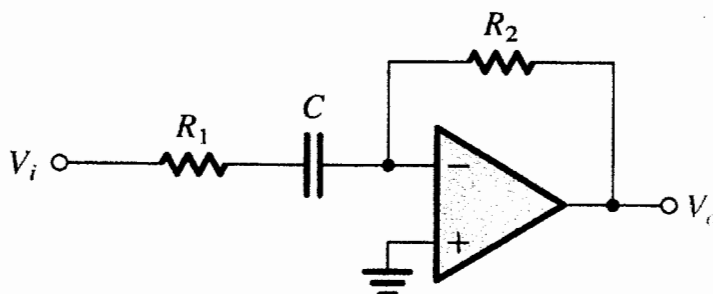


Fig. 1

2. It is required to design the active-loaded differential MOS amplifier of Fig. 2 to obtain a differential gain of  $50\text{ V/V}$ . The technology available provides  $\mu_n C_{ox} = 4\mu_p C_{ox} = 400\ \mu\text{A/V}^2$ ,  $|V_t| = 0.5\text{ V}$ , and  $|V_A'| = 20\text{ V}/\mu\text{m}$  (channel length modulation effect) and  $V_{DD} = V_{SS} = 1\text{ V}$ . Use a bias current  $I = 200\ \mu\text{A}$  and operate all devices at  $|V_{OV}| = 0.2\text{ V}$  (overdrive voltage).
  - (1) Find the  $W/L$  ratios of the four transistors ( $Q_1$ ,  $Q_2$ ,  $Q_3$ , and  $Q_4$ ). (4%)
  - (2) Specify the channel length required of all transistors. (4%)
  - (3) If  $I$  is delivered by a simple NMOS current source operated at the same  $V_{OV}$ , for  $V_{CM} = 0$ , what is the allowable range of  $v_o$ ? (4%)

(背面仍有題目, 請繼續作答)

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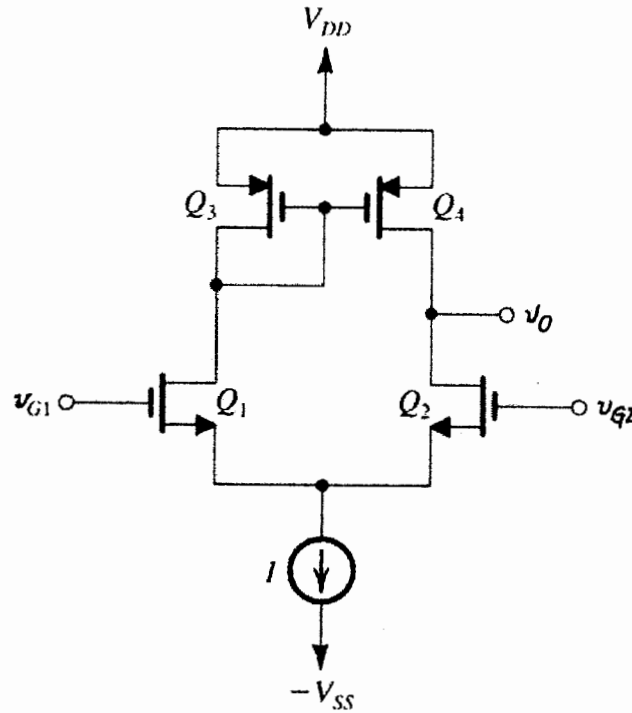


Fig. 2

3. The open-loop gain of an amplifier has break frequencies at  $f_{p1}=100$  kHz,  $f_{p2}=200$  kHz, and  $f_{p3}=1$  MHz. The low-frequency (or DC) gain is  $A_o=800$ , and the feedback factor is  $\beta=0.5$ . Please calculate
  - (1) The gain crossover frequency. (4%)
  - (2) The phase margin. (4%)
  
4. An amplifier with open-loop voltage gain of  $10^4$  and poles at  $10^3$  Hz,  $10^5$  Hz, and  $10^6$  Hz is to be compensated by the addition of a dominant pole to operate stably with a closed-loop gain of 30 dB with a  $45^\circ$  phase margin, what new pole frequency should be used? (6%)

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5. (1) A second-order filter has the transfer function

$$T(S) = \frac{1}{S^2 + (10 + \alpha)S + 25}$$

Find the range of  $\alpha$  for which the filter can operate stably? (4%)

- (2) What type of this filter can be realized as the following transfer function?

Explain why? (8%)

$$T(S) = \frac{S(S^2 + 0.01)(S^2 + 4)}{(S^2 + 0.8S + 0.52)(S^2 + 0.56S + 0.18)(S^2 + 0.56S + 0.86)}$$

6. A waveform generator circuit is shown in Fig. 6. If the op amps have saturation voltages of  $\pm 10$  V, given  $C = 0.01$  m F,  $R_1 = 10$  k $\Omega$ ,  $R_2 = 20$  k $\Omega$ , and  $R = 50$  k $\Omega$ .

- (1) Sketch and label the waveforms  $v_1$  and  $v_2$ . (10%)  
 (2) Determine the frequency of waveform  $v_1$ . (5%)

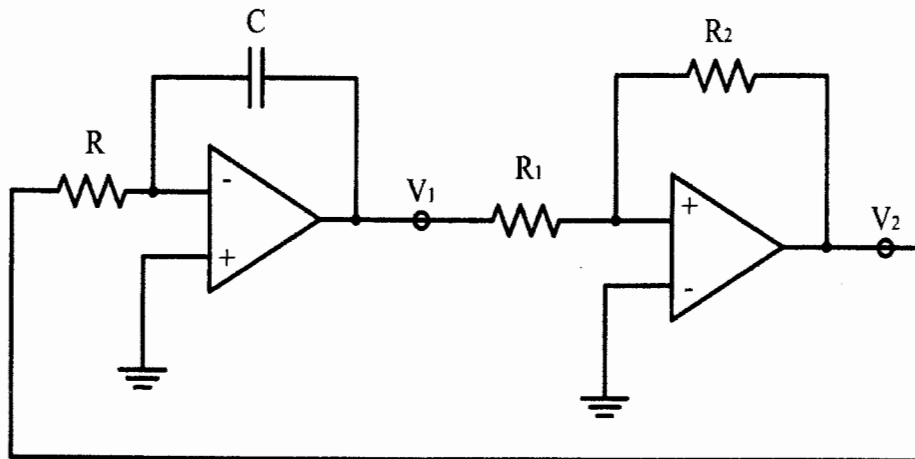


Fig. 6

7. Consider the circuit shown in Fig. 7 with parameters of  $v_i = 5 \times \sin(\omega t)$  volts where  $\omega = 2000\pi$  radians/sec,  $C_1 = C_2 = 1\mu$ F and uncharged initially, the cut-in voltage of both diodes  $V_\gamma$  while the forward diode resistance  $r_f = 0\Omega$ , reverse breakdown voltage = 100 V, saturation current =  $2.5 \times 10^{-9}$  A.

(背面仍有題目,請繼續作答)

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(1) What are the maximum and minimum voltage of  $v_o$  when  $V_f = 0$  for Fig. 7(a)?

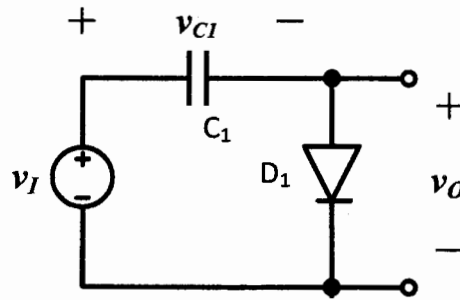
(4%)

(2) Assume  $V_f = 0$  for Fig. 7(a). Sketch waveforms of  $v_{C1}$  and  $v_o$  along with

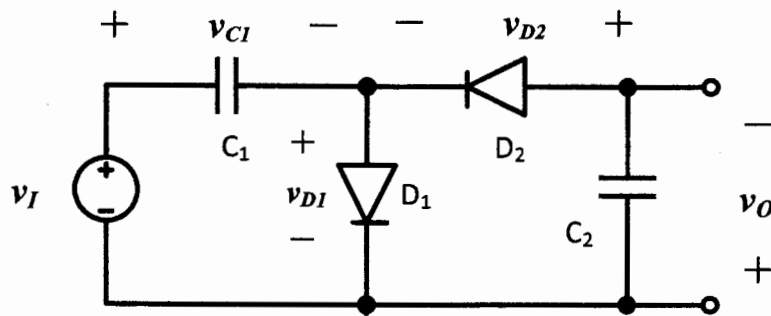
$v_I$  starting from  $t = 0$  sec to 3 ms. (10%)

(3) Assume  $V_f = 0.7$  V for Fig. 7(b). What are the maximum and minimum voltage

of  $v_o$ ? (4%)



(a)



(b)

Fig. 7

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8. Consider the circuit shown in Fig. 8 with parameters of  $V_{DD}=5\text{ V}$ ,  $\mu_n C_{ox}=40\ \mu\text{ A/V}^2$ , and  $\mu_p C_{ox}=20\ \mu\text{ A/V}^2$ ,  $V_{tn}=|V_{tp}|=1\text{ V}$ ,  $(W/L)_{Q1}=(W/L)_{Q3}=2\ \mu\text{ m}/1\ \mu\text{ m}$ ,  $(W/L)_{Q2}=(W/L)_{Q4}=4 \times (W/L)_{Q1}$ ,  $(W/L)_{Q5}=(W/L)_{Q6}=(W/L)_{Q7}=(W/L)_{Q8}$ . Note that  $B$  and  $\bar{B}$  are outputs while  $Set$ ,  $Reset$ , and  $Clk$  are inputs.  $Clk$  is the clock signal.  $Set$  and  $Reset$  are complementary signals, i.e., when  $Set = V_{DD}$ ,  $Reset = 0$ ; vice versa.

- (1) Determine the minimum  $W/L$  for both  $Q_5$  and  $Q_6$  required to ensure that the two back-to-back inverters of the circuit will switch at half of  $V_{DD}$  when inputs  $Set$  and  $Clk$  are  $V_{DD}$ . (7%)
- (2) Find the minimum  $W/L$  for both  $Q_5$  and  $Q_6$  such that switching is achieved when inputs  $Set$  and  $Clk$  are half of  $V_{DD}$ . (8%)

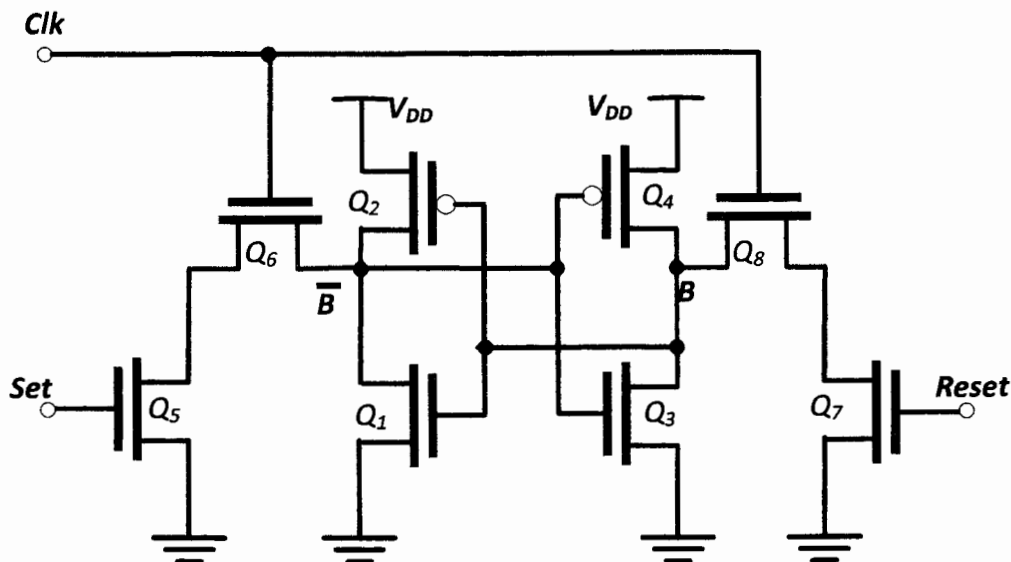


Fig. 8