

編號：187,198,205

國立成功大學 104 學年度碩士班招生考試試題

系所組別：電機工程學系甲乙丁戊組、電腦與通信工程研究所丙丁組、電機資訊學院-微電奈米聯招

考試科目：電子學

考試日期：0211，節次：1

第1頁，共5頁

※ 考生請注意：本試題可使用計算機。 請於答案卷(卡)作答，於本試題紙上作答者，不予計分。

1. In the circuit shown in Fig. 1, both diodes are identical, conducting 10 mA at 0.7 V and 100 mA at 0.8 V. For $V_O = 80 \text{ mV}$, find the value of R . Given the thermal voltage $V_T = 25 \text{ mV}$. (10%)

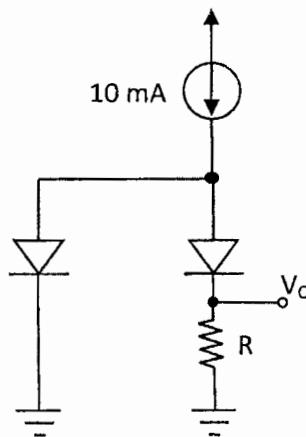


Fig. 1

2. In the circuit shown in Fig. 2, v_{sig} is a small sinewave signal with zero average. Given the transistor $\beta = 100$, $r_o = 200 \text{ k}\Omega$, and $R_C = 20 \text{ k}\Omega$.

- (a) Find R_E for a dc emitter current of 0.5 mA. (5%)
(b) Find the (small-signal) voltage gain. (8%)

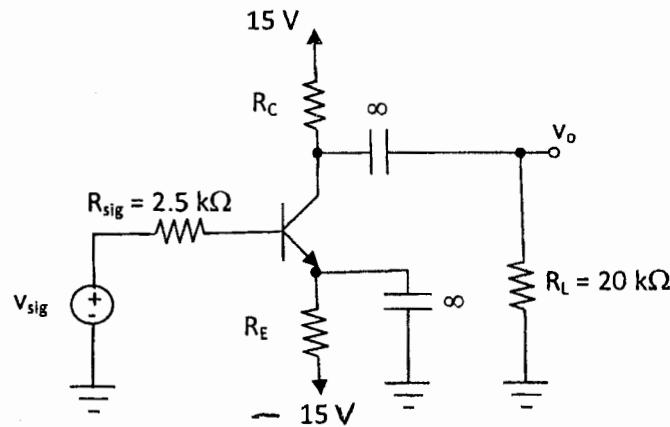


Fig. 2

3. In the circuit shown in Fig. 3, the two transistors have equal lengths ($L_1 = L_2$) but widths related by $W_2/W_1 = 5$. Design the circuit to obtain $I_O = 0.5 \text{ mA}$. Let $k_n'(W/L)_1 = 0.8 \text{ mA/V}^2$, $V_t = 1 \text{ V}$, and $\lambda = 0$.

- (a) Find the required value of R . (5%)
(b) What is the lowest possible V_O while Q_2 remains in the saturation region? (5%)

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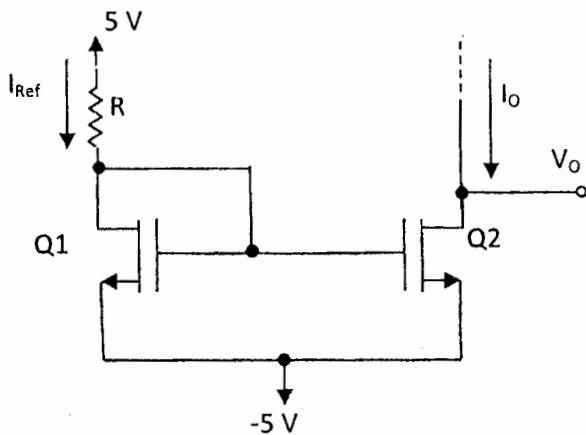


Fig. 3

4. Fig. 4 show a series-shunt amplifier in which the three MOSFETs are sized to operate at $|V_{ov}|=0.2$ V. Let $|V_t|=0.5$ V, $|V_A|=20$ V, $I=0.1\text{mA}$, $R_1=2\text{k}\Omega$, and $R_2=18\text{k}\Omega$. The current sources utilize single transistors and thus have output resistances equal to r_o .
- (a) Calculate the overall open-loop voltage gain A . (4%)
 - (b) Find feedback factor β . (3%)
 - (c) Find closed-loop gain $A_f=V_o/V_s$. (3%)
 - (d) Find the output resistance R_{out} . (3%)

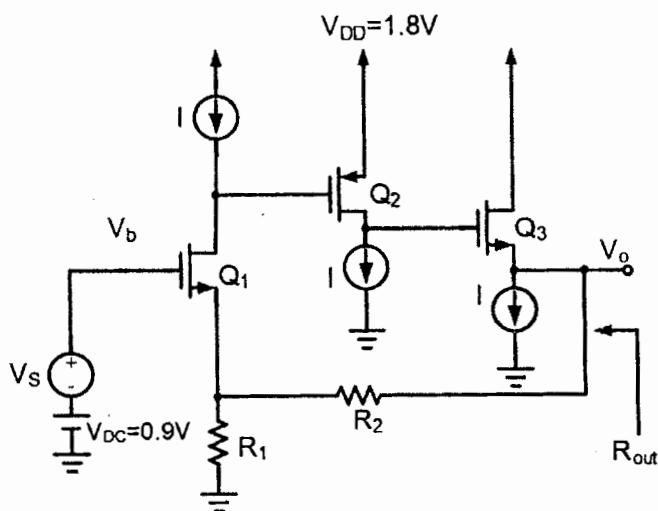


Fig. 4

5. For the cascaded gain stage in Fig. 5, let $2I=26\mu\text{A}$; $\mu_n C_{ox}=20 \mu\text{A}/\text{V}^2$; $\mu_p C_{ox}=10\mu\text{A}/\text{V}^2$; $|V_t|=1\text{V}$; $|V_A|=26\text{V}$; W/L for Q_1 , Q_2 , Q_{1C} , and $Q_{2C}=130/8$; W/L for Q_{3C} and $Q_{4C}=65/8$; and W/L=8/8 for Q_3 and Q_4 .
- (a) Find output impedance, R_o (5%)
 - (b) Find voltage gain, $A=V_o/(V_{in^+}-V_{in^-})$ (5%)

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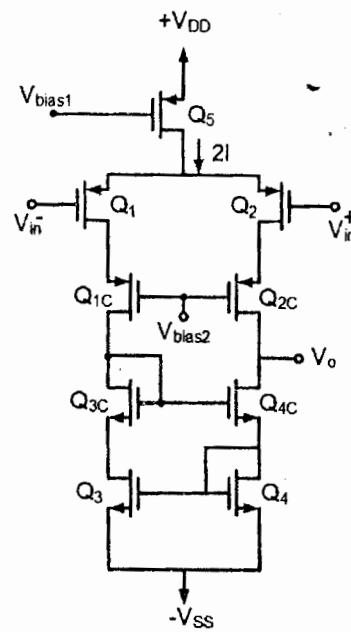


Fig. 5

6. The NMOS transistor in the discrete CS amplifier circuit of Fig. 6 is biased to have $g_m = 1 \text{ mA/V}$. Find the three poles (ω_{p1} , ω_{p2} , ω_{p3}) relative to $0.01 \mu\text{F}$, $0.1 \mu\text{F}$, $10 \mu\text{F}$ and the gain (A_M) in the transfer function of

$$\frac{V_o}{V_{sig}} = A_M \left(\frac{s}{s + \omega_{p1}} \right) \left(\frac{s}{s + \omega_{p2}} \right) \left(\frac{s}{s + \omega_{p3}} \right) \quad \text{where } \omega_{pi} = 2\pi f_i$$

(10%)

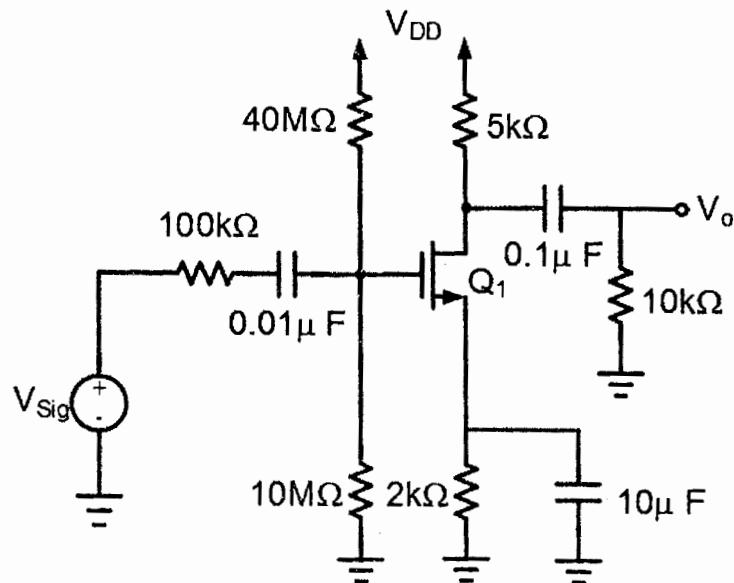


Fig. 6

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7. For the circuit shown in Fig. 7, assuming the threshold voltages of all transistors to be equal in magnitude and $k_1=k_2, k_3=k_4=16k_1$. (Note that $k = \frac{1}{2} \mu_{ox} \frac{W}{L}$). Find the required value of I_1 to yield a bias current in Q_3 and Q_4 of 1.6 mA. (6%)

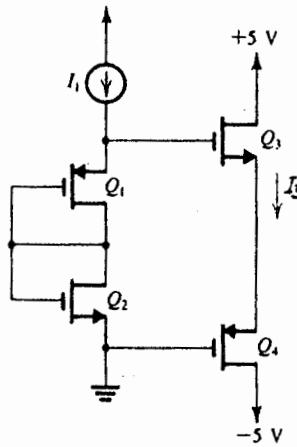


Fig. 7

8. For the circuit shown in Fig. 8, assuming that the op amplifier is ideal.

- (a) Derive the expression of voltage transfer ratio $\frac{v_o}{v_s}$ as a function of ω . (4%)
- (b) Sketch the magnitude Bode plot to scale. (4%)
- (c) For design requirements of DC gain=2 and cutoff frequency= 500Hz, find the values of R_2 and C , assume $R_1=1\text{ k}\Omega$. (4%)

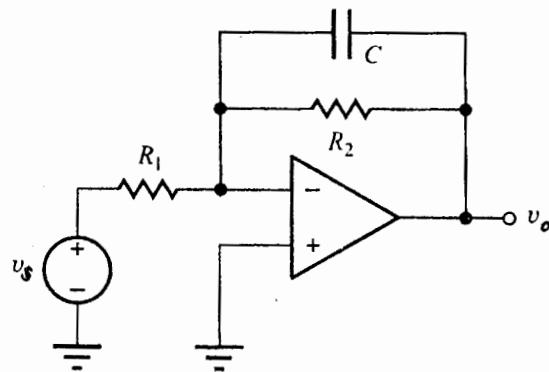


Fig. 8

9. Consider the circuit illustrated in Fig. 9.

- (a) Find the minimum value of R_2/R_1 required for oscillation. (4%)
- (b) Find the frequency of oscillation. (4%)

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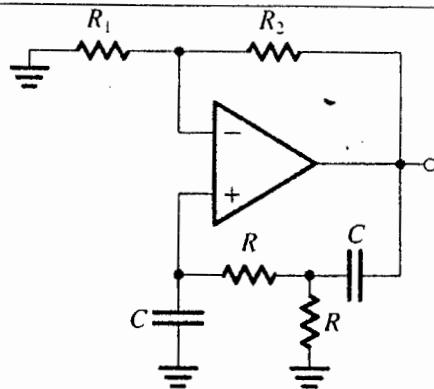


Fig. 9

10. Fig. 10 shows a circuit that performs signal generation.

- Draw the waveforms of v and v_o . (4%)
- What is its frequency of oscillation? (4%)

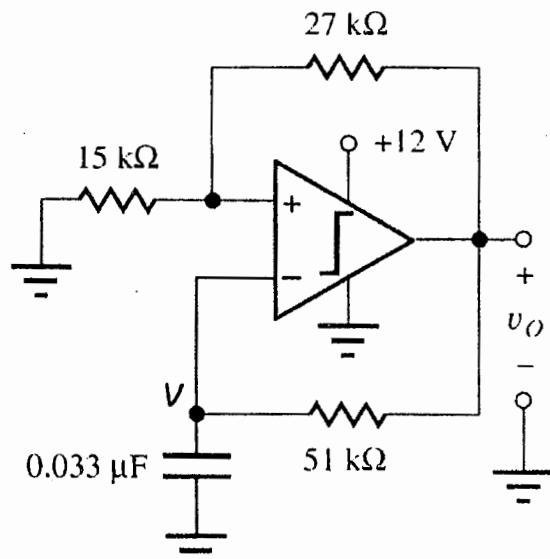


Fig. 10