編號： 188

國立成功大學 105 學年度碩士班招生考試試題

系　　所：電腦與通信工程研究所

考試科目：計算機組織與作業系統

考試日期：0228，節次：1

※ 考生請注意：本試題不可使用計算機。　請於答案卷(卡)作答，於本試題紙上作答者，不予計分。

1. What is the context switch time, associated with swapping, if a disk drive with a transfer rate of 2 MB/s is used to swap out part of a program that is 400 KB in size? Assume that no seeks are necessary and that the average latency is 15 ms. The time should reflect only the amount of time necessary to swap out the process.(10%)

2. Describe how a safe state ensures deadlock will be avoided.(10%)

3. Why is it important for the scheduler to distinguish I/O-bound programs from CPU-bound programs? (10%)

4. A system with two dual-core processors has four processors available for scheduling. A CPU-intensive application is running on this system. All input is performed at program start-up, when a single file must be opened. Similarly, all output is performed just before the program terminates, when the program results must be written to a single file. Between startup and termination, the program is entirely CPU-bound. Your task is to improve the performance of this application by multithreading it. The application runs on a system that uses the one-to-one threading model (each user thread maps to a kernel thread).
   (1) How many threads will you create to perform the input and output?(5%)
   (2) How many threads will you create for the CPU-intensive portion of the application? Explain.(5%)

5. (1) What is the purpose of system call?(5%)
   (2) What are the advantages and disadvantages of using the same system call interface for manipulating both files and devices?(5%)

6. Design a direct memory access (DMA) controller.
   a. Show a detailed block diagram of a DMA controller, including registers used.(10%)
   b. Describe the operation of the DMA controller. (10%)

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7. Show the design of the following memory hierarchy system for a conventional five-stage pipeline processor. Assume both the virtual address and physical address are 32 bits. The page size is 4KB. The L1 ITLB has 48 entries and is 3-way set associative. The L1 DTLB is direct-mapped and has 32 entries. The L2 TLB is a unified TLB which has 128 entries using 4-way set associative design. The data cache and instruction cache are both physically addressed; each has a cache size of 64KB, direct-mapped, line size 32 bytes.

   a. Show the L1 ITLB design and explain the translation of virtual address to the physical address for ITLB. 10%
   b. Show the L1 DTLB design integrated with the data cache. 10%
   c. Show how to integrate the three TLBs, instruction cache, and the data cache to the pipeline. 10%