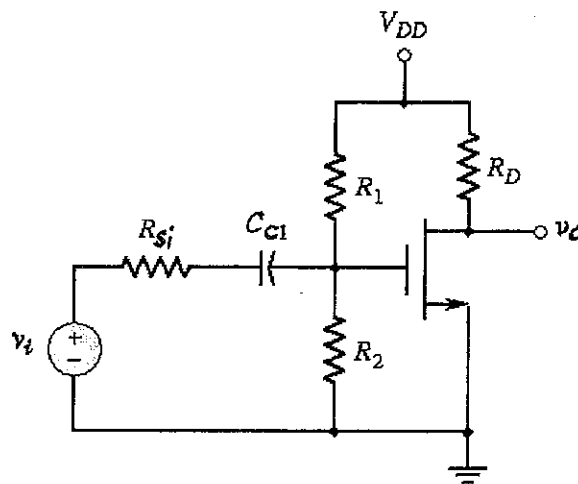
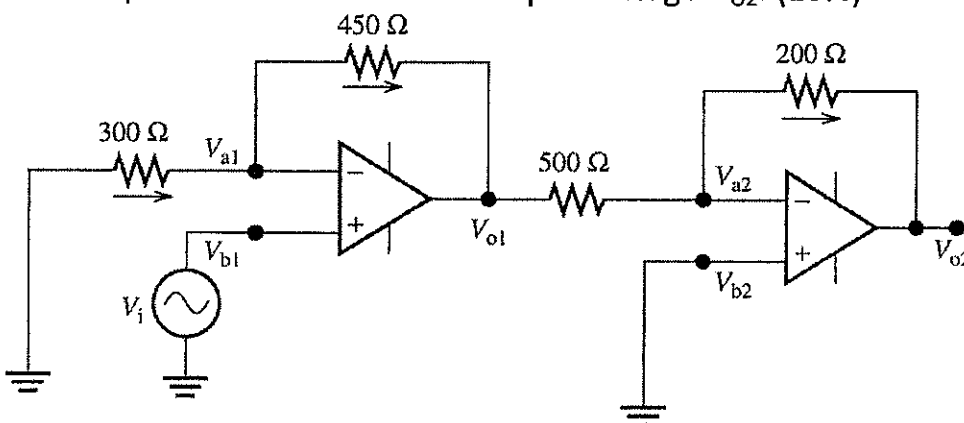


※考生請注意：本試題可使用計算機。請於答案卷(卡)作答，於本試題紙上作答者，不予計分。

1. A Zener diode has an equivalent series resistance of  $20\ \Omega$ . If the voltage across the Zener diode is  $5.20\ \text{V}$  at  $I_z = 1\ \text{mA}$ , determine the voltage across the diode at  $I_z = 10\ \text{mA}$ . (10%)
2. Consider an n-channel MOSFET with parameters  $V_{TN} = 1\ \text{V}$ ,  $\mu_n C_{ox} = 40\ \mu\text{A}/\text{V}^2$ , and  $W/L = 40$ . Assume the transistor is biased in saturation region, and the drain current is  $I_D = 1\ \text{mA}$ . Calculate the transconductance ( $g_m$ ) (10%).
3. For the circuit shown below, the parameters are:  $V_{DD} = 10\ \text{V}$ ,  $R_1 = 70.9\ \text{k}\Omega$ ,  $R_2 = 29.1\ \text{k}\Omega$  and  $R_D = 5\ \text{k}\Omega$ . The transistor parameters are:  $V_{TN} = 1.5\ \text{V}$ ,  $K_n = 0.5\ \text{mA}/\text{V}^2$ , and  $\lambda = 0.01\ \text{V}^{-1}$ . Assume  $R_{si} = 4\ \text{k}\Omega$ . Determine the small-signal voltage gain (10%), input resistance (5%) and output resistance (5%) of the common-source amplifier.



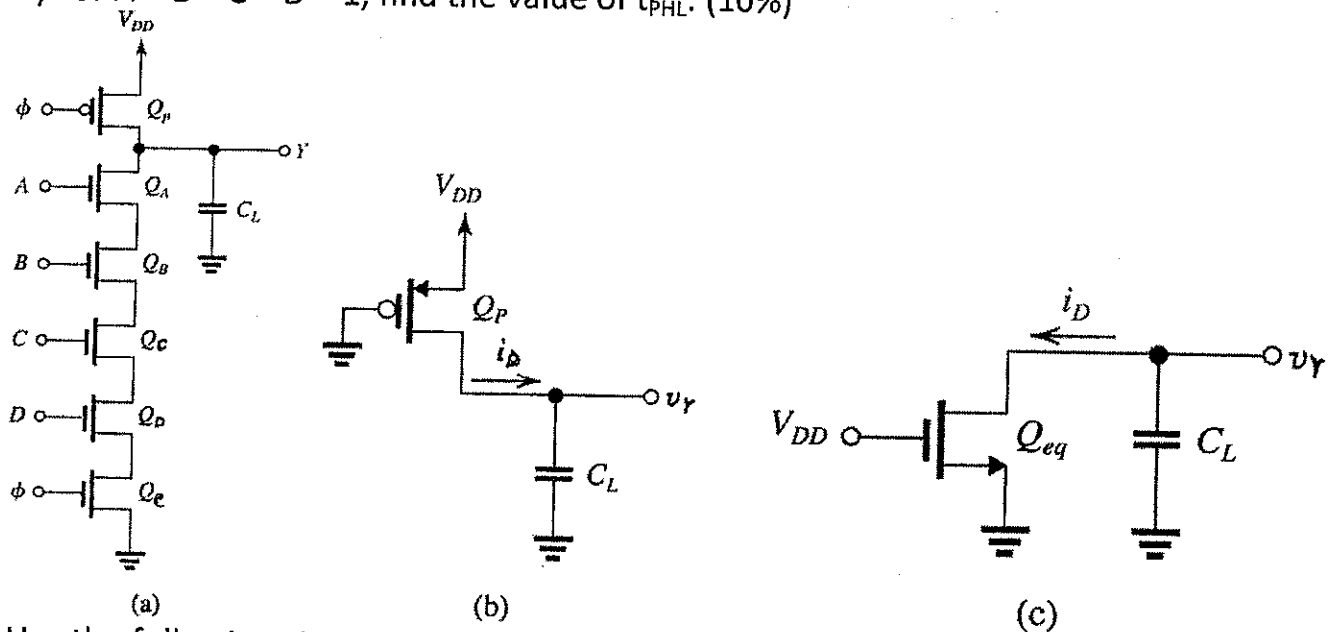
4. Consider a bipolar transistor that has parameters  $f_T = 500\ \text{MHz}$  at  $I_C = 1\ \text{mA}$ ,  $\beta_0 = 100$ , and  $C_\mu = 0.3\ \text{pF}$ . Calculate the bandwidth  $f_\beta$  (10%) and capacitance  $C_\pi$  (10%).
5. Given  $V_i = 20\ \text{V}$ . Determine the output voltage  $V_{O2}$ . (10%)



6. Consider the four input dynamic-logic NAND gate shown below. Assume the gate is fabricated in a  $0.18 \mu\text{m}$  technology for which  $V_{DD} = 1.8 \text{ V}$ ,  $V_t = 0.5 \text{ V}$ , and  $\mu_n C_{ox} = 4\mu_p C_{ox} = 300 \mu\text{A/V}^2$ . To keep  $C_L$  small, NMOS devices with  $W/L = 0.27 \mu\text{m}/0.18 \mu\text{m}$  are used. The PMOS precharge transistor  $Q_p$  has  $W/L = 0.54 \mu\text{m}/0.18 \mu\text{m}$ . The total capacitance  $C_L$  is found to be  $20 \text{ fF}$ .

i) Consider the precharge condition (figure (b)) with the gate of  $Q_p$  at  $0 \text{ V}$ , and assume that at  $t = 0$ ,  $C_L$  is fully discharged. Calculate the rise time of the output stage, defined as the time for  $v_Y$  to rise from 10% to 90% of the final voltage  $V_{DD}$ . (10%)

ii) For  $A = B = C = D = 1$ , find the value of  $t_{PHL}$ . (10%)



7. Use the following circuit to realize a second-order low pass function of the maximally flat type with a 3 dB frequency of  $100 \text{ kHz}$ . Let  $R = 1 \text{ k}\Omega$ . Find the values of  $L$  and  $C$ . (10%)

