編號: 188、199、204

## 國立成功大學 107 學年度碩士班招生考試試題

系 所:電機工程學系、電腦與通信工程研究所、電和資訊、學院一個電、茶料解認

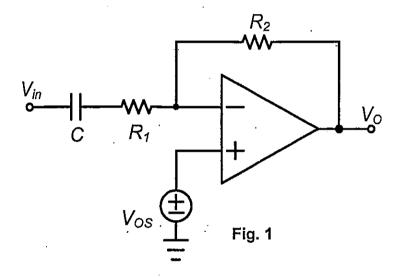
考試科目:電子學

考試日期:0205,節次:1

第1頁,共4頁

※ 考生請注意:本試題可使用計算機。 請於答案卷(卡)作答,於本試題紙上作答者,不予計分。

- 1. Consider an inverting amplifier with a nominal gain of 1000 constructed from an op amp with an input offset voltage of 4 mV and with output saturation levels of  $\pm 12$  V which is shown in Fig. 1.
  - (a) What is the dc offset voltage at the output? (4%)
  - (b) What (approximately) is the peak sine-wave signal that can be applied at the input without output clipping? (4%)
  - (c) If  $R_1 = 1 \text{ k}\Omega$  and  $R_2 = 1 \text{ M}\Omega$ , find the value of the coupling capacitor C that will ensure that the gain will be greater than 57 dB down to 100 Hz? (4%)



- 2. For the bridge-rectifier circuit of Fig. 2, use the constant-voltage-drop diode model with  $V_D$ =0.7 V. Consider  $V_S$ =12-V (rms) sinusoid and R=100  $\Omega$ .
  - (a) Find the average (or dc component) of the output voltage ? (4%)
  - (b) Find the peak diode current? (4%)
  - (c) Find the peak inverse voltage (PIV) of diode D<sub>3</sub> ?(4%)

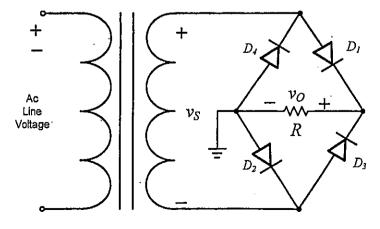


Fig. 2

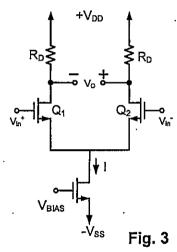
編號: 188、199、204 國立成功大學 107 學年度碩士班招生考試試題

系 所:電機工程學系、電腦與測信工程研究所、電機資訊學院一做電、奈米斯格

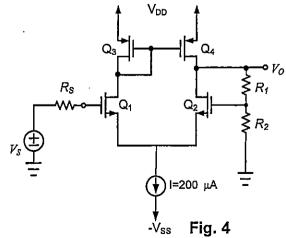
系 所· 电機工程学系、医的图像和像2012-00(新广)、图像 图87(多)、不断的图像,不不断的图像 考試科目:電子學 考試科目:電子學 考試科目:

第2頁,共4頁

- 3. A MOSFET differential amplifier shown in Fig. 3 is biased with a current source I=400  $\mu$ A. The transistors have W/L=16,  $k_n$  =400  $\mu$ A/V²,  $V_A$ =20 V.  $C_{gs}$ =40 fF,  $C_{gd}$ =5 fF, and  $C_{db}$ =5 fF. The drain resistors are 10  $k\Omega$  each. Also, there is a 100-fF capacitive load between each drain and ground.
  - (a) Find the transconductance, gm (4%)
  - (b) Find the differential gain, A<sub>d</sub> (4%)
  - (c) If the input signal source has a small resistance  $R_{sig}$  and thus the frequency response is determined primarily by the output pole, estimate the 3-dB frequency  $f_H$ . (4%)
  - (d) If, in a different situation, the amplifier is fed symmetrically with a signal source of 40 k $\Omega$  resistance (i.e., 20 k $\Omega$  in series with each gate terminal), use the open-circuit time-constants method to estimate  $f_H$  (4%)



- 4. The current-mirror-loaded differential amplifier in Fig. 4 has a feedback network consisting of the voltage divider ( $R_1$  and  $R_2$ ), with  $R_1+R_2=1$  M $\Omega$  and the bias current of I=200  $\mu$ A. The devices are sized to operate at  $|V_{OV}|=|V_{GS}-V_{TH}|=0.2$  V. For all devices,  $|V_A|=10$  V. The input signal source has a zero dc component.
  - (a) Find the open-loop gain of A (3%) according to the loop gain AB
  - (b) Find the feedback factor  $\beta$  (3%), the values of  $R_1$  and  $R_2$  that result in a closed-loop gain of exactly 5 V/V (4%)



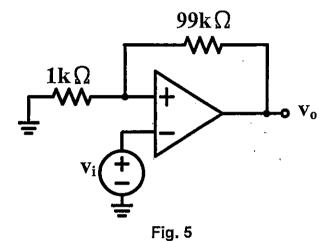
編號: 188、1912~4 國立成功大學 107 學年度碩士班招生考試試題

系 所:電機工程學系、電腦板直信工程不中的可、电视發訊管院一份地、京米斯·根

考試科目:電子學 考試日期:0205,節次:1

## 第3頁,共4頁

- 5. For the circuit shown in Fig. 5, assuming the operational amplifier is ideal with +12V and -12V output saturation levels.
  - (a) What are the name and function of this circuit? (4%)
  - (b) Sketch and label the Vo-V1 transfer characteristic of this circuit. (3%)
  - (c) For a 200mV-amplitude sine-wave input with zero average, draw and label the waveform of  $V_0$ ? (3%)



- 6. For the circuit schematic of a 2-stage CMOS operational amplifier shown in Fig. 6, assuming  $V_{DD}$ =1.5V,  $-V_{SS}$ =-1.5V,  $V_{tn}$ =[ $V_{tp}$ ]=0.5V, and all transistors are operated with overdrive voltage of 0.2V magnitude.
  - (a) Find its input common-mode range. (3%)
  - (b) Find its allowed range for Vo. (3%)
  - (c) What is the function of capacitor C<sub>C</sub>? (4%)

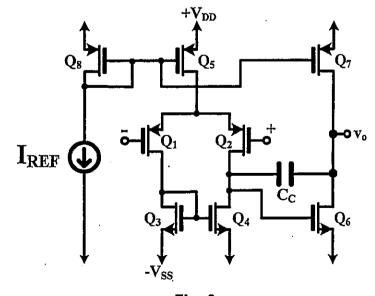


Fig. 6

編號: 188、199、204 國立成功大學 107 學年度碩士班招生考試試題

系 所:電機工程學系、電腦細胞で程。研究所、電机変列学院一般也、茶米斯招

考試科目:電子學 考試日期:0205,節次:1

第4頁,共4頁

7. An amplifier has the following voltage transfer function:

$$A(s) = \frac{10000}{(1 + \frac{s}{10^2})(1 + \frac{s}{10^6})}$$

- (a) Draw the asymptotic Bode plots of A (magnitude and phase). (6%)
- (b) If this amplifier is connected with unity negative feedback (i.e.,  $\beta$ =1), find the resulted phase margin. (4%)
- 8. For the circuit shown in Fig. 7, assuming the diodes ( $D_1$  and  $D_2$ ) have the same junction area as the transistors ( $Q_N$  and  $Q_P$ ),  $V_{CC}$ =12V,  $I_{BIAS}$ =1 mA,  $R_L$ =100 $\Omega$ ,  $\beta_N$ =50, and  $|V_{CE}|$ =0.2V.
  - (a) What are the name and function of this circuit? (4%)
  - (b) What is the quiescent current (i.e, at  $V_0 = 0V$ ) of  $Q_N$  and  $Q_P$ ? (4%)
  - (c) What are the largest possible positive and negative output signal levels? (4%)
  - (d) To achieve a positive peak output level equals to the negative peak level, what value of I<sub>BIAS</sub> is required? (4%)
  - (e) For the IBIAS value found in (d), what does the quiescent current become? (4%)

