國立成功大學 109 學年度碩士班招生考試試題

系　　所：電腦與通信工程研究所

考試科目：電子學

考試日期：0211，節次：1

※ 考生請注意：本試題可使用計算機。　請於答案卷(卡)作答，於本試題紙上作答者，不予計分。

1. Fig. 1 shows the inverting amplifier with an ideal opamp. Use this circuit to design an inverting amplifier with a gain of 100 and an input resistance of 1MΩ. Assume that for practical reasons it is required no to use resistors greater than 1MΩ. (12%)
   (a) Derive an expression for the closed-loop gain v_O/v_I of the circuit (4%)
   (b) If $R_1=R_2=R_4$, find the required values, R_1 and R_3, to fit the gain of 100. (8%)

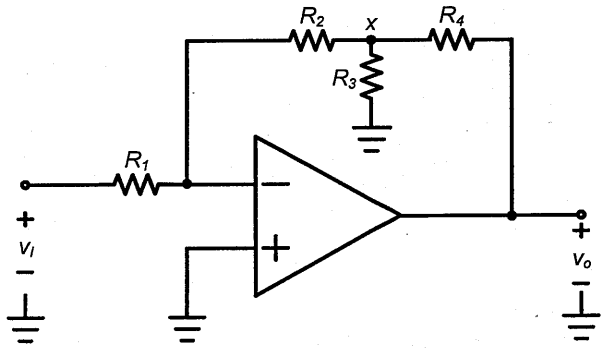

Fig. 1

2. Consider a common-emitter circuit using a BJT as shown in Fig. 2 having $I_S=10^{-15}$A, a collector resistance $R_C=6.8k\Omega$, and a power supply $V_{CC}=10V$. (12%)
   (a) Determine the value of the bias voltage V_{BE} required to operate the transistor at $V_{CE}=3.2V$. What is the corresponding value of I_C? (4%)
   (b) If an input sine-wave signal of 5-mV peak amplitude is superimposed on V_{BE}, find the amplitude of the output sine-wave signal (assume linear operation) (4%)
   (c) Find the positive increment in v_{BE} (Δv_{BE} above V_{BE}) that drives the transistor to the edge of saturation, where $v_{CE}=0.3V$ (4%)

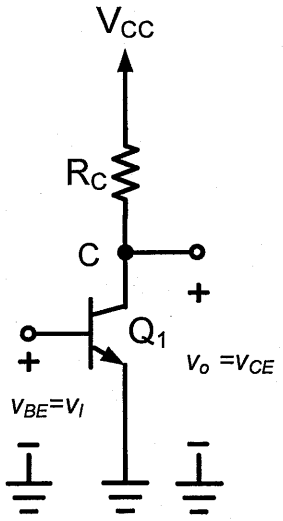

Fig. 2

國立成功大學 109 學年度碩士班招生考試試題

系　　所：電腦與通信工程研究所

考試科目：電子學

考試日期：0211，節次：1

3. A bipolar differential amplifier (Fig. 3) utilizes a single CE transistor current source to supply a bias current I of 200 μA, and simple current-source loads formed by pnp transistors. For all transistors, β=100 and early voltage $|V_A|$=10 V. (12%)

   (a) Find differential gain A_d ($A_d = \frac{v_{o2}-v_{o1}}{v_{i1}-v_{i2}}$) (4%)

   (b) Find input impedance R_{id} (4%)

   (c) If the two load transistors exhibit a 1% mismatch in their r_o's, find CMRR (4%)

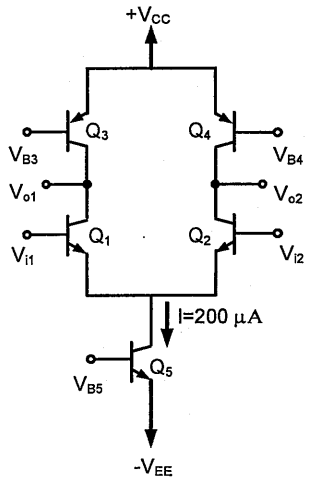

Fig. 3

4. Fig. 4 shows a common-source amplifier biased by a constant-current source I. Let R_{sig}=0.5 MΩ, R_G=2 MΩ, g_m=3 mA/V, R_D=20 kΩ, and R_L=10 kΩ. (14%)

   (a) Find the midband gain A_M (2%)

   (b) Find the values of bypass and coupling capacitors (C_S, C_{C1}, C_{C2}) to locate the three low-frequency poles at 100 Hz, 10 Hz, and 1 Hz. Using a minimum total capacitance, with the capacitors specified only to a single significant digit. (12%)

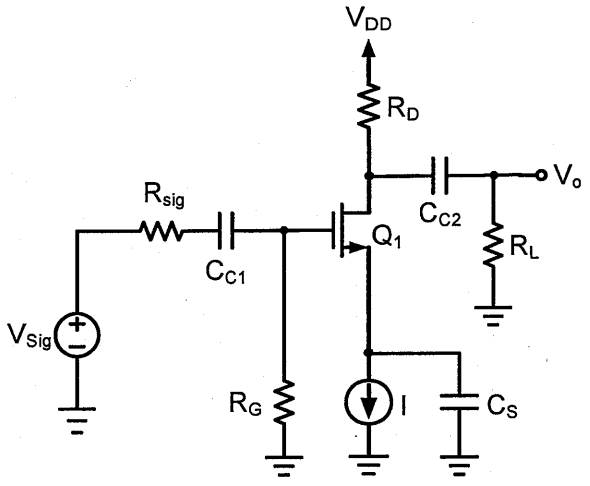

Fig. 4

5. (15%)

(a) Fig. 5(a) shows the Antoniou inductance-simulation circuit. Assume the op amps are ideal. What is the equivalent inductance L seen from the node 1 (as depicted). (5%)

(b) Based on 5(a), please find the transfer function, $V_o(s)/V_i(s)$, for the circuit shown in Fig. 5(b)? (5%)

(c) Based on 5(b), please explain why the circuit shown in Fig.5(c) is an all pass filter. [Hint: complementary circuit] (5%)

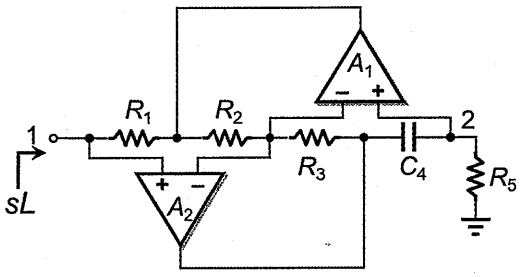

Fig. 5(a)

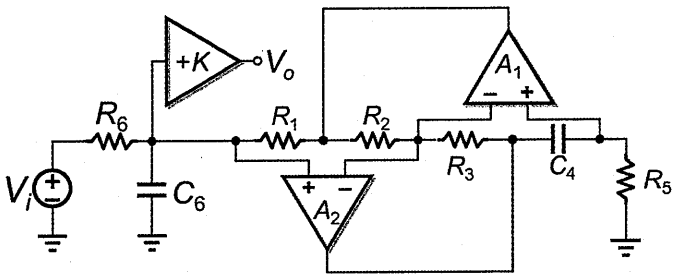

Fig. 5(b)

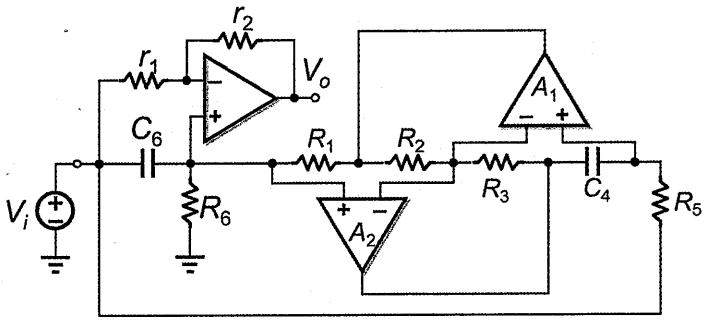

Fig. 5(c)

6. Design the cross-coupled LC oscillator of Fig. 6 to operate at a resonance frequency ω_0 = 10 Grad/s. The inductors available have inductance L = 10 nH and quality factor Q = 10. If the transistor output resistance r_o = 1 kΩ, find the required value of C and the minimum required value of g_m at which Q_1 and Q_2 are to be operated. (10%)

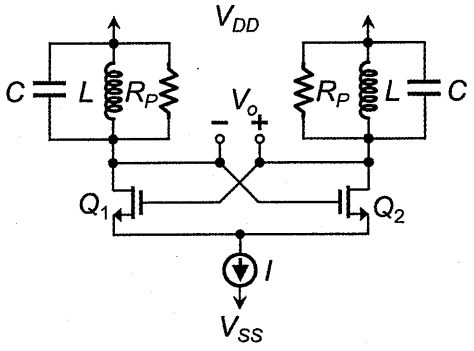

Fig. 6

國立成功大學 109 學年度碩士班招生考試試題

系　　所：電腦與通信工程研究所

考試科目：電子學

考試日期：0211，節次：1

7. For the amplifier whose open-loop transfer function $A(s)$ is depicted in Fig. 7, to what value must the first pole frequency be lowered to obtain stable performance for the cases of (10%)
   (a) $\beta = 0.001$ and (5%)
   (b) $\beta = 0.1$? (5%)
   Assume only the first pole is changed and the other poles are remain the same.

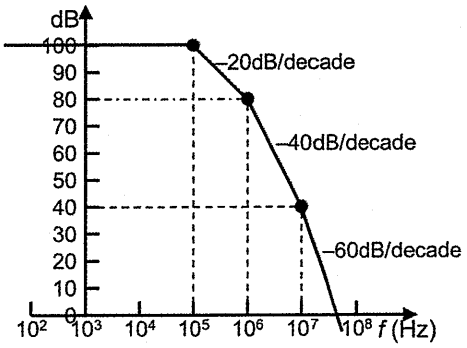

Fig. 7

8. For the two-stage op amp and its small signal model shown in Fig. 8. (15%)
   (a) Given a nonzero R_C (M16 biased in triode region), please drive the expression of zero frequency in terms of g_{mi}, R_i, and C_i. (5%)
   (b) There are several possibilities to choose R_C when compensating the op amp. Please state "two" reasonable approaches in choosing the value of R_C, and give their corresponding expression of R_C. (10 %)

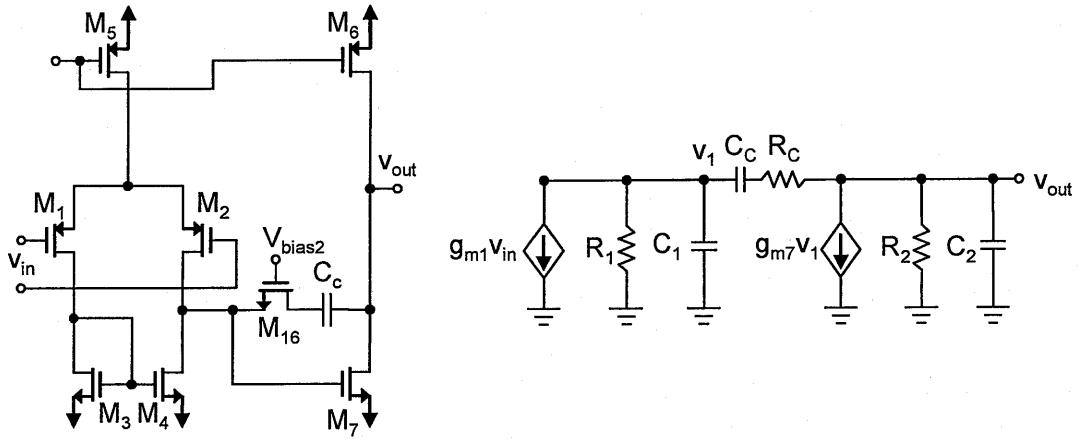

Fig. 8