國立成功大學

110學年度碩士班招生考試試題

編　號： 192

系　所： 電腦與通信工程研究所

科　目： 電子學

日　期： 0203

節　次： 第 1 節

備　註： 可使用計算機

國立成功大學 110 學年度碩士班招生考試試題

系　所：電腦與通信工程研究所

考試科目：電子學　　　　考試日期：0203，節次：1

※ 考生請注意：本試題可使用計算機。　請於答案卷(卡)作答，於本試題紙上作答者，不予計分。

1. Derive the transfer function of the circuit in Fig. 1 with an ideal op amp and show that it can be written in the form $\frac{V_O}{V_i} = -\frac{R_2/R_1}{[1+(\omega_1/j\omega)][1+(j\omega/\omega_2)]}$

   (a) Assume that the circuit is designed such that $\omega_2 >> \omega_1$, what are the ω_1 and ω_2 ? (4%)

   Find approximation expressions for the transfer function (V_o/V_i) in the following frequency regions:

   (b) $\omega << \omega_1$ (4%)

   (c) $\omega_1 << \omega << \omega_2$ (4%)

   (d) $\omega >> \omega_2$ (4%)

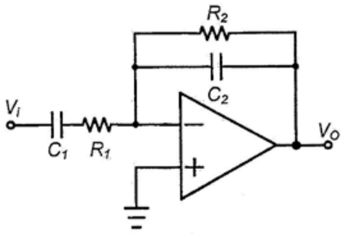

Fig. 1

2. A current-mirror-loaded MOS differential amplifier as shown in Fig. 2 is biased with a current source I=0.2mA. The two NMOS transistors of the differential pair are operating at overdrive voltage: $V_{ov}=V_{GS}-V_{tn}=0.2V$, and the PMOS device of the mirror are operating at overdrive voltage: $|V_{ov}|=|V_{GS}|-|V_{tp}|=0.2V$. The Early voltage $V_{An}=|V_{AP}|=10V$. Assume $C_m=0.1$ pF and $C_L=0.2$ pF.

   (a) Find the dc gain of current-mirror-loaded MOS differential amplifier? (4%)

   (b) Find the frequencies of the poles (f_{P1}, f_{P2}) and zero (f_z) of the current-mirror-loaded MOS differential amplifier? (12%)

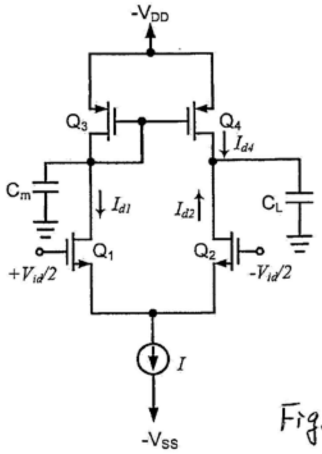

Fig. 2

3. The transconductance amplifier in Fig. 3 utilizes a differential amplifier with gain μ and a very high input resistance. The differential amplifier drives a transistor Q characterized by its g_m and r_o. A resistor R_F senses the output current I_o. The open loop gain and closed loop gain are A and A_f, respectively, and the feedback factor is β.
   (a) For $A\beta >> 1$, select a value for R_F that results in $A_f \equiv I_o/V_s \cong 5$ mA/V.(2%)
   (b) Find the circuit and derive an expression for A.(4%)
   (c) Find A and A_f with μ=1000 V/V, g_m=2 mA/V, r_o=20 kΩ, and the value of R_F you selected in (a). (4%)
   (d) Find values of R_o and R_{of}. (8%)

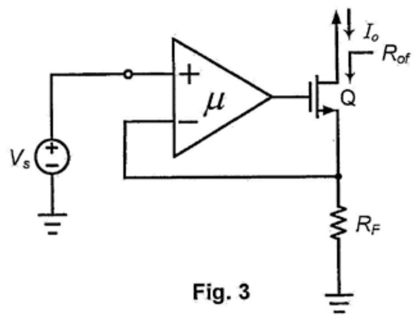

Fig. 3

4. For a dc voltage of 1V applied to the input of the switched-capacitor Filter shown in Fig. 4, in which C_1 is 1 pF, C_2 is 10 pF, and the frequency of the non-overlapping clocks (ϕ_1 and ϕ_2) is 100 kHz.
   (a) What charge is transferred for each cycle of the two-phase clock? (2%)
   (b) What is the average current drawn from the input source? (2%)
   (c) What change would you expect in the output for each cycle of the clock? (3%)
   (d) What is the average slope of the staircase output voltage produced? (3%)

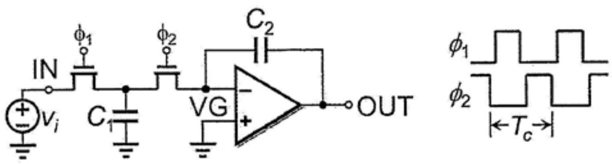

Fig. 4

5. [Butterworth Filter Approximation]

(a) Find the Butterworth transfer function that meets the following low-pass filter specifications: passband edge frequency f_p = 10 kHz, stopband edge frequency f_s = 40 kHz, maximum allowed variation in passband transmission A_{max} = 1 dB, minimum required stopband attenuation A_{min} = 28 dB, and dc gain = 2. (15 %)

(b) Follow (a), if A_{min} is to be exactly 28 dB, to what value can A_{max} be reduced. (5 %)

Some equations you may need during answering this question: $A(\omega_s) = 10\log\left[1+\epsilon^2\left(\frac{\omega_s}{\omega_p}\right)^{2N}\right]$ $\left[1+\epsilon^2\left(\frac{\omega_s}{\omega_p}\right)^{2N}\right]$; $\epsilon = \sqrt{10^{A_{max}/10}-1}$; $\omega_0 = \omega_p(1/\epsilon)^{1/N}$; and $T(s) = \frac{K\omega_0^N}{(s-p_1)(s-p_2)\cdots(s-p_N)}$

6. An op amp with an open-loop voltage gain of 80 dB and poles at 10^5 Hz, 10^6 Hz, and 2×10^6 Hz is to be compensated to be stable for **unity** β. Assume that the op amp incorporates an amplifier equivalent to that in Fig. 5, with C_1 = 150 pF, C_2 = 5 pF, and g_m = 40 mA/V, and that f_{p1} is caused by the input circuit and f_{p2} by the output circuit of this amplifier. Assume that R_1 and C_1 represent the total resistance and capacitance between node G and ground, and R_2 and C_2 represent the total resistance and capacitance between node D and ground, although they are not depicted here. If the target phase margin is 45°, please find the required value of the compensating Miller capacitance and the new frequency of the output pole. (20%)

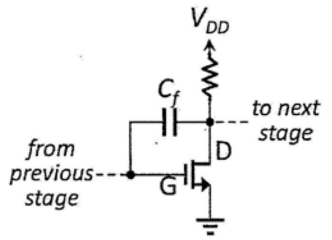

Fig. 5