國立成功大學

114學年度碩士班招生考試試題

編　號：133、142、145

系　所：電機工程學系
電腦與通信工程研究所
電機資訊學院-微電、奈米聯招

科　目：電子學

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節　次：第 1 節

注　意：1.可使用計算機
2.請於答案卷(卡)作答，於試題上作答，不予計分。

1. The common-source (CS) amplifier in Fig. 1 is biased to operate at g_m=5 mA/V, and has the following component values: R_{sig}=100 kΩ, R_{G1}=47 MΩ, R_{G2}=10 MΩ, C_{C1}=0.01 μF, R_S=2 kΩ, C_S=10 μF, R_D=4.7 kΩ, R_L=10 kΩ, and C_{C2}=1 μF. Neglect r_o and find (a) gain (A_M=V_o/V_{sig}), (b) input pole (f_{P1}), (c) source pole (f_{P2}), (d) source zero (f_Z), (e) output pole (f_{P3}), and (f) -3dB frequency (f_L). (30%)

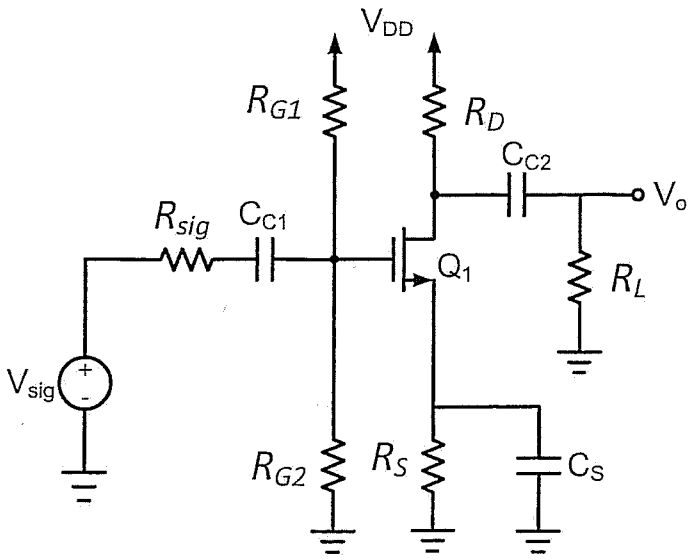

Fig. 1

2. The circuit in Fig. 2 utilizes a voltage amplifier with gain μ in a shunt-shunt feedback topology with a feedback network composed of resistor R_F=20 kΩ, input resistor R_S=2 kΩ, and load resistor R_L= ∞.
   (a) If the amplifier μ has a DC gain of 10^3 V/V, an input resistance R_{id}=100 kΩ, and an output resistance r_o=2 kΩ, find the actual V_o/V_S realized. Also, find R_{in} and R_{out}. (15%)
   (b) If the amplifier μ has an upper -3dB frequency of 1 KHz and a uniform -20-dB/decade gain rolloff, what is the 3-dB frequency of the gain |V_o/V_S |. (5%)

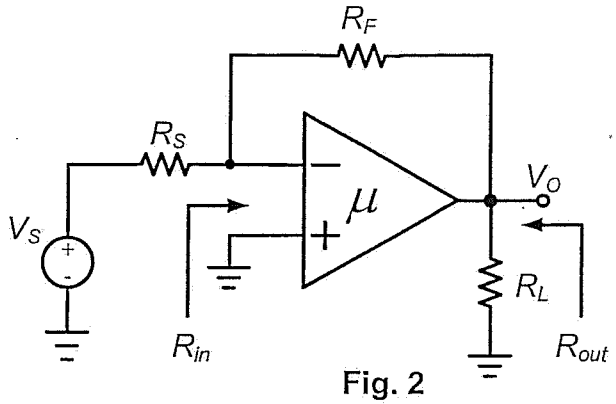

Fig. 2

3. Please design a two-stage CMOS op amp, as shown in Fig. 3, for obtaining a dc gain of 4000 V/V. Assume that the available fabrication technology is of the 0.5-μm type for which $V_{tn} = |V_{tp}| = 0.5$ V, $k_n' = 200$ μA/V², $k_p' = 80$ μA/V², $V'_{An} = |V'_{Ap}| = 20$ V/μm, and $V_{DD} = |V_{SS}| = 1.65$V. To achieve a reasonable dc gain per stage, use $L = 1$ μm for all devices. Also, for simplicity, operate all devices at the same $|V_{OV}|$, in the range of 0.2 V to 0.4 V. The current is given to be $I = 200$ μA and $I_{D6} = 500$ μA, and C_C is 1.8 pF.
Please give the values realized for the following parameters (4% each)
(a) input common-mode range,
(b) maximum possible range of the output swing,
(c) output resistance R_o,
(d) common-mode rejection ratio (CMRR),
(e) power-supply rejection ratio PSRR+,
(f) power-supply rejection ratio PSRR–,
(g) slew rate (SR),
(h) unit-gain frequency (ft).

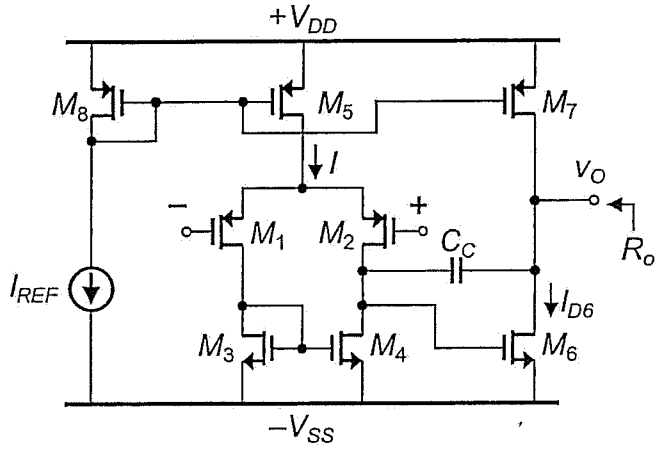

Fig. 3

4. For the quadrature oscillator shown in Fig. 4, please briefly answer the questions (a)-(f), (3% each)
(a) What is the function of the circuit enclosed in the dash-circle line 1?
(b) What is the function of the circuit enclosed in the dash-circle line 2?
(c) What is the function of the circuit enclosed in the dash-circle line 3?
(d) Which value of R_f should we use for maintaining the oscillation?
(e) Follow 4(d), what is the oscillation frequency ω_0?
(f) What is the phase difference of the sinusoidal signals of v_{o1} and v_{o2}?

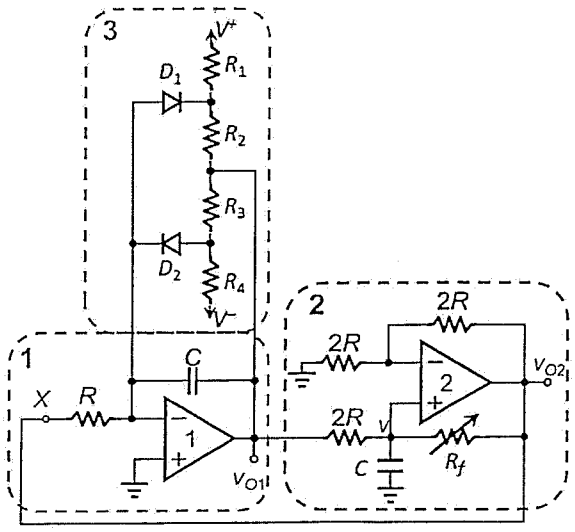

Fig. 4