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1. A low-power Schottky TTL logic circuit is shown in Fig. 1. Assume a transistor current gain of β=30 for all transistors. **(a)** Calculate the maximum fanout for $v_X = v_Y = 3.6$V. **(b)** Using the results of part (a), determine the power dissipated in the circuit for $v_X = v_Y = 3.6$V. (If the turn-on voltages of p-n junction and Schottky diode are 0.7V and 0.3V, respectively.) (18%)

2. What is the logic function at Y as implemented by the circuit in Fig. 2? (7%)

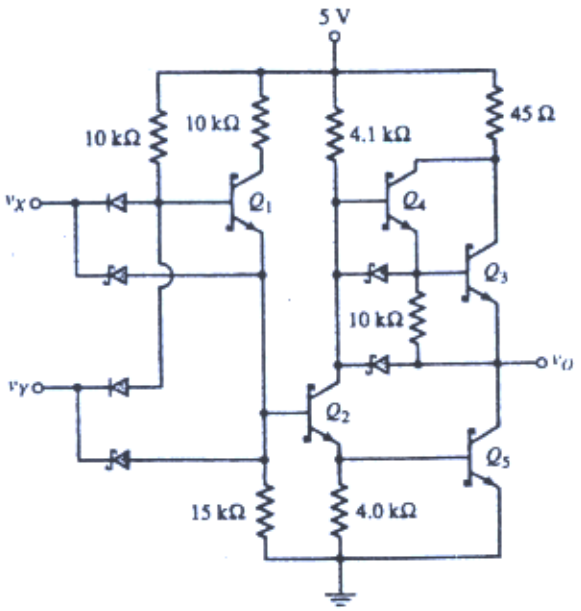

Fig. 1

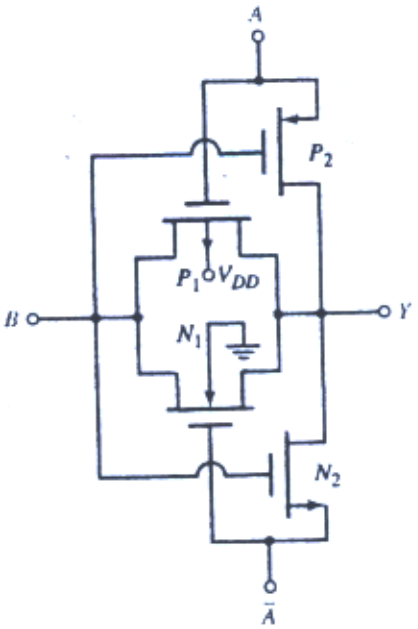

Fig. 2

(背面仍有題目,請繼續作答)

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3. The amplifier shown in Fig.3 (a) is biased to operate at I_D=1mA and g_m=1mA/V. R is 50kΩ. Assume the transistor is ideal.

(a) Find the midband gain. (5%)

(b) Find the value of C_S that place the corresponding pole at 10 Hz. What's the frequency of the transfer-function zero introduced by C_S? (5%)

(c) Given an expression for the gain function of $v_o(s)/v_i(s)$. What is the gain of the amplifier at dc? (5%)

(d) Using the FET high frequency equivalent model shown in Fig.3 (b), find the upper 3-dB frequency and unity gain frequency, assume C_{gs}=C_{gd}=1pF, r_o=∞. (5%)

(e) Plot the Bode diagram including the amplitude and phase. Indicate the key parameters in the figure. (5%)

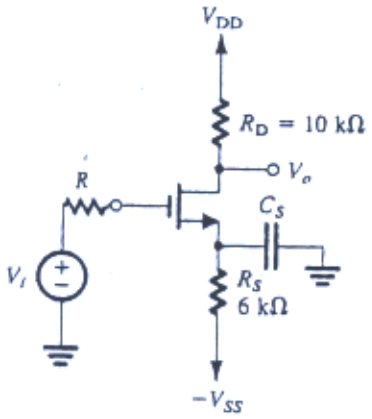

Fig. 3(a)

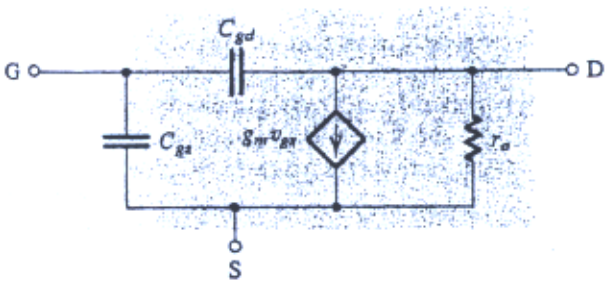

Fig.3 (b)

4. The open-loop gain of a feedback amplifier is given by:

$$A(s)=\frac{10^6}{\left(1+\frac{s}{10^2}\right)\left(1+\frac{s}{10^5}\right)\left(1+\frac{s}{10^7}\right)}$$

(a) Draw the asymptotic Bode diagram of A. (15%)

(b) What is the phase margin if the amplifier is connected in negative feedback with $\beta = 1$? (5%)

(c) What is the critical value of β to reach the range from which the closed-loop feedback amplifier can be stable (assuming that β is frequency-independent) ? (5%)

5. (a) Explain briefly the reason why BJT and MOSFET can amplify signals. (5%)

(b) State the possible mechanism that is responsible for the saturated $i_C - v_{CE}$ and $i_D - v_{DS}$ characteristics of BJT and MOSFET, respectively. (5%)

(c) For the amplifier shown in Fig. 4, draw the possible load line of Q_1 and voltage transfer ($v_O - v_I$) curve. Assume Q_1 and Q_2 are two matched enhancement-type MOSFETs. (5%)

(d) Derive the dc and small-signal output resistance R_o for the circuit shown in Fig. 5. Assume $r_o \neq \infty$. (10%)

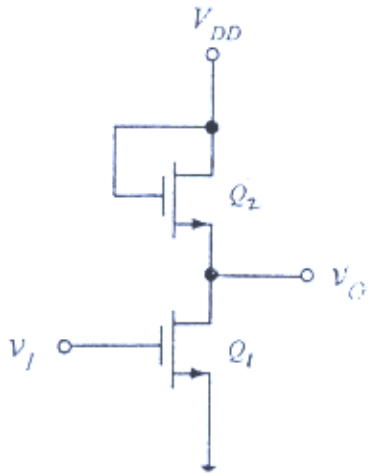

Fig. 4

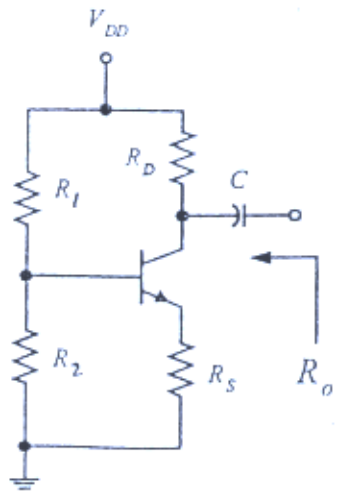

Fig. 5