

Choose the correct answers for the following multiple choice problems. Each question may have more than one answer. 5 point each, no partial point, no penalty.

1. Which of the following is (are) true?
 - (a) For a fixed size cache memory, the larger the line size is the smaller the tag memory the cache uses.
 - (b) For a fixed size cache memory, the larger the line size is the larger the tag memory the cache uses.
 - (c) For a direct-mapped cache, no address tag is the same in the tag memory.
 - (d) For a two-way associative cache, no address tag is the same in the tag memory.
2. Which of the following is (are) true for a 64KB cache with a line size of 32 bytes? Assume that the cacheable memory is 1 GB.
 - (a) In a direct-mapped implementation, the tag length is 16 bits; the index field is 11 bits in length.
 - (b) In a direct-mapped implementation, the tag length is 14 bits; the index field is 16 bits in length.
 - (c) In a direct-mapped implementation, the tag length is 14 bits; the field determining line size is 5 bits in length.
 - (d) In a two-way implementation, the tag length is 15 bits; the index field is 10 bits in length.
3. Which of the following is (are) true?
 - (a) A non-blocking cache allows hit under miss to hide miss latency.
 - (b) A non-blocking cache does not allow miss under hit to hide miss latency.
 - (c) Miss under miss allows multiple outstanding cache misses.
 - (d) A non-blocking cache allows a load instruction to access the cache if the previous load is a cache miss.

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4. Which of the following is (are) true for the forwarding unit in a 5-stage pipelined processor?
 - (a) The forwarding unit is used to detect the instruction cache stalling.
 - (b) The forwarding unit is a combinational circuit which detects the true data dependency for EXE pipeline stage and selects the forwarded results for the execution unit.
 - (c) The forwarding unit is a pipeline register which detects the true data dependency for EXE pipeline stage and selects the forwarded results for the execution unit.
 - (d) The forwarding unit compares the source register number of the instructions in the MEM and WB stages with the destination register number of the instruction in the decode stage.

5. Which of the following is (are) not true?
 - (a) A control hazard is the delay in determining the proper data to load in the MEM stage of a pipeline processor.
 - (b) A load-use data hazard occurs because the pipeline flushes the instructions behind.
 - (c) To flush instructions in the pipeline means to load the pipeline with the requested instructions using the predicted PC.
 - (d) A branch prediction buffer is a buffer that the compiler uses to predict a branch.

6. Which of the following is (are) true for the combinations of events in the TLB, virtual memory system, and cache?
 - (a) It is possible that an access results in a TLB hit, a page table hit, and a cache miss.
 - (b) It is possible that an access results in a TLB hit, a page table miss, and a cache miss.
 - (c) It is possible that an access results in a TLB hit, a page table miss, and a cache hit.
 - (d) It is possible that an access results in a TLB miss, a page table hit, and a cache miss.

7. Which of the following is (are) true?
 - (a) Virtual memory technique treats the main memory as a fully-set associative write-back cache.
 - (b) Virtual address must be always larger than the physical address.
 - (c) TLB can be seen as the cache of a page table.
 - (d) If the valid bit for a virtual address is off, a page fault occurs.

8. Which of the following is (are) true?
- (a) Memory-mapped I/O is an I/O scheme in which special designed I/O instructions are used to access the memory space.
 - (b) The process of periodically checking status bits to see if it is time for the next I/O operation is called interrupt.
 - (c) DMA is a mechanism that provides a device controller the ability to transfer data directly to or from memory without involving the processor. DMA is also a bus master.
 - (d) In a cache-based system, because of the coherence problem, thus DMA can not be used.
9. Which of the following is (are) true?
- (a) Computers have been built in the same, old-fashioned way for far too long, and this antiquated model of computation is running out of steam.
 - (b) $\text{Dynamic power} = \text{Capacitive load} \times \text{Voltage}^2 \times \text{Frequency switched}$
 - (c) Static power is due to the small operating current in CMOS.
 - (d) Yield = the percentage of good dies from the total number of dies on the wafer.
10. Which of the following is (are) true?
- (a) ISA (instruction set architecture) is an abstraction which is the interface between the hardware and the low-level software (assembly instructions). This abstract interface enables different implementations of the same ISA to run identical software.
 - (b) A caller is the program that is called by the procedure which gives the call.
 - (c) A basic block is a sequence of instructions with branch at the beginning and at the end.
 - (d) A register file is a large memory for storing files.
11. Which of the following statements conforming to the design principle: simplicity favors regularity?
- (a) Keeping all instructions in a single size.
 - (b) Always requiring three operands in arithmetic instructions
 - (c) Keeping the register fields in the same place in each instruction format
 - (d) Having the same opcode field in the same place in each instruction format.
12. Which of the following is (are) true?
- (a) Page fault is signaled by software.
 - (b) TLB exception can only be handled in hardware.
 - (c) A cache miss is handled in hardware.
 - (d) A page fault is handled in software.

(背面仍有題目,請繼續作答)

13. Which of the following is (are) true?
- (a) When a cache write hit occurs, the written data are also updated in the next level of memory. This is the write-through policy.
 - (b) There is no cache coherency problem for the write-through cache since the data are written into the next level of memory.
 - (c) When a cache write hit occurs, the written data are only updated in the cache. This is the write-back policy.
 - (d) Cache data inconsistency appears in a write-back cache when an I/O master writes data into the memory block which is cached.
14. Which of the following affects the CPI (clock per instruction)?
- (a) Cache structure
 - (b) Memory data bus width
 - (c) Process technology
 - (d) Clock cycle time
15. Which of the following is (are) true?
- (a) A C compiler compiles a C program into assembly language program for the target machine.
 - (b) Pseudoinstructions are instructions which are not implemented in hardware.
 - (c) A label is a pseudoinstruction.
 - (d) Pseudoinstructions are directives in an assembly language program.
16. Which of the following is (are) true?
- (a) In a pipeline processor, a structure hazard means that the hardware cannot support the combination of instructions that are executed in the same clock cycle.
 - (b) A structure hazard is caused by the branch instruction which is mispredicted.
 - (c) A structure hazard occurs if a unified cache is accessed both by the instruction fetch and the data load at the same clock.
 - (d) A structure hazard is an exception which causes the processor to fetch instruction from the exception handler.
17. Which of the following is (are) true?
- (a) Pipelining reduces the instruction execution latency to one cycle.
 - (b) Pipelining not only improves the instruction throughput but also the instruction latency.
 - (c) Pipelining improves the instruction throughput rather than individual instruction execution time.
 - (d) Pipelining improves the instruction throughput other than individual instruction execution time.

18. Which of the following is (are) true?
- (a) Temporal locality means the tendency to use data items that are close in location.
 - (b) Temporal locality means the tendency to reuse data items that are recently accessed.
 - (c) Spatial locality means the tendency to use data items that are close in location.
 - (d) Spatial locality means the tendency to reuse data items that are recently accessed.
19. Which of the following is (are) data transfer instructions?
- (a) jal subroutine_1
 - (b) sw R1, 100(R2)
 - (c) beq R1, R2, start
 - (d) or R1, R2, R3
20. Which of the following instruction(s) performs NOT operation assuming R0 = 0?
- (a) OR R1, R0, R3
 - (b) AND R1, R0, R3
 - (c) NOR R1, R0, R3
 - (d) ADD R1, R0, R3