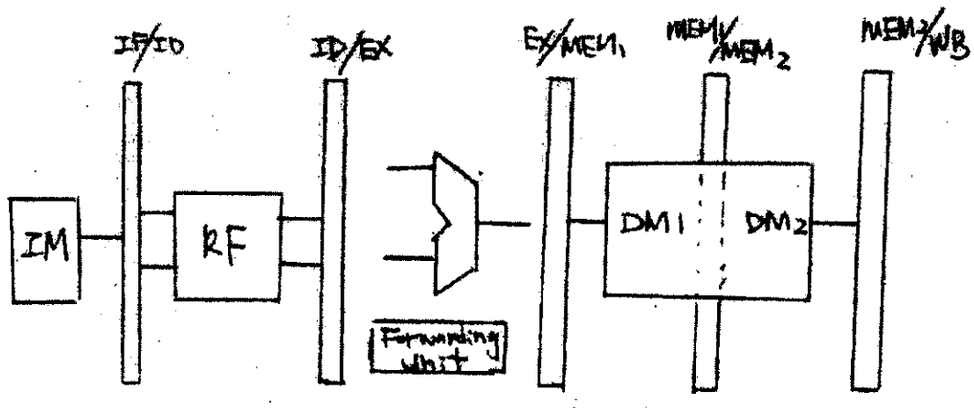
1. For the pipeline processor shown below, the following sequence of instructions causes the pipeline hazard due to load-use dependency.
lw $4, 100($2)
add $8, $4, $4.
Assuming the lw instruction will take 2 data memory cycles to get the data from the memory and a forwarding circuit is employed, detail the design of the hazard detection unit for this processor assuming MIPS-like ISA is used. Sketch your design in the processor pipeline diagram and explain the signals you use (10%). Write down the behavioral code for the logic of the hazard detection unit (20%).



2. For the above pipelined processor, come up with the behavioral code for the logic of the forwarding unit assuming MIPS-like ISA is used. State you assumptions if any. (20%)

（背面仍有題目，請繼續作答）

3. [40 points] Assume you are asked to design the architecture of the memory hierarchy for a computer which has a 32-bit MIPS processor with a clock rate of 2 GHz. The processor has a 32 KB (Kilo-Byte) 1st level cache and a 256 KB 2nd level cache on chip. The 1st level cache is 4-way associative and the 2nd level cache is fully associative. Assume the word size is 32 bits and the block size for both caches is 32 bytes. The size of the physical memory is 2 GB (Giga-Byte). The memory space is byte-addressing. Based on the given information, please answer the following questions.

   (a) [12 points] How many bits are needed for each of the fields in the following structure to index 1st level cache and the 2nd level cache, respectively? Note show the answers for 1st level cache and 2nd level cache separately.

Tag	Index	Block Offset

   (b) [10 points] Suppose the access time to main memory with 2nd level cache disabled is 250ns. That is, the access time includes 1st level miss handling. Suppose the base CPI of the processor is 2, assuming all references hit in the 1st level cache. Further assume the test program you use to test the memory hierarchy has a 3% miss rate per instruction for 1st level cache. Now with 2nd level cache enabled, the test program has a miss rate of 0.2%. Suppose the access time of 2nd level cache is 20ns for either a hit or a miss. How much performance improvement you will get with the 2nd level cache enabled?

   (c) [10 points] Suppose this computer has a 32-bit virtual address space and 4 KB page size.

      i. [3 points] How many virtual pages are there?
      ii. [3 points] How many physical pages are there?
      iii. [4 points] Assume each entry in a page table consume 1 word, what is the size of the page table in bytes?

   (d) [8 points] Following the specification in (c), given the page table in the following, please derive the physical address of the virtual address 0x0000 1004, and then locate the address in the 1st level cache. That is, show which set the address will be if it's in 1st level cache.

Page Entry no	Valid	Dirty	Ref	Physical page address
0	1	1	1	0x0001 1000
1	1	0	0	0x0004 1000
2	1	0	0	0x0001 2000
3	1	1	1	0x0003 3000
4	1	0	1	0x000F E000
….	…	…	…	……

4. [10 points] Suppose you run photoshop to load a 4 MB (Mega-Byte) image file from the hard disk to the memory for editing. Unfortunately, your disk is so fragmented that all data blocks associated with this file is scattered around the disk randomly. The parameters of the disk are listed below.

   Average seek time: 12 milli-second
   Rotational speed: 5000 RPM (rotation per minute)
   Block size: 512 bytes
   Transfer rate: 0.4 MB/sec
   Ignore all other overheads

   How long does the photoshop program need to wait for the file transfer to finish from the hard disk to the memory?