

系所組別： 電腦與通信工程研究所甲組

考試科目： 計算機組織與作業系統

考試日期： 0307，節次： 1

※ 考生請注意：本試題 可 不可 使用計算機

1. Design a cache for the following cases. Show the block diagram of the design, including buses used for the cache, the tag memory, data memory, and how the address to the cache is used. The cache size is 16K-bytes for all cases.
 - a. A direct-mapped cache with 32-bytes of the line size. 10%
 - b. A four-way set associative cache with 64-bytes of the line size. 10%
 - c. Compute the tag memory size in bits of the caches in (a) and (b) respectively. 10%

2. True or false 2% each
 - a. A blocking cache allows a load instruction to access the cache if the previous load is a cache miss which is still in progress.
 - b. A load-use data hazard occurs because the pipeline flushes the instructions behind.
 - c. It is possible that an access results in a TLB hit, a page table hit, and a cache miss.
 - d. It is impossible that an access results in a TLB hit, a page table miss, and a cache hit.
 - e. It is impossible that an access results in a TLB miss, a page table hit, and a cache hit.
 - f. Checking the status bit of an I/O address to see if it is time for the next I/O operation is called interrupt.
 - g. A system using a write-through cache as its private cache will not have cache coherence problem since the written data are also updated in the main memory.
 - h. When an interrupt occurs, the processor must always respond to the interrupt and enter the interrupt service routine.
 - i. ISA (instruction set architecture) is an abstraction that enables different implementations of the same ISA for the processor, for example, a pipelined implementation or a non-pipelined one.
 - j. A page fault is signaled by a system call.

(背面仍有題目,請繼續作答)

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3. System calls can be grouped roughly into five major categories: _____, _____, _____, _____, and _____. 5%
4. When an interrupt occurs, the system needs to save the current context of the process currently running on the CPU to restore that context when the processing is done. The context is represented in the _____ of the process; it includes the value of the _____, _____, and _____. 4%
5. The benefits of multithreaded programming can be broken down into four major categories: 1. _____, 2. _____, 3. _____, 4. _____. 4%
6. A deadlock situation can arise if the following four conditions hold simultaneously in a system: 1. _____, 2. _____, 3. _____, 4. _____. 4%
7. The binding of instructions and data to memory addresses can be done at any step along the way: _____, _____, _____. 3%
8. Consider the following four processes, with the length of the CPU burst given in milliseconds: 20%

<u>Process</u>	<u>Arrival Time</u>	<u>Burst Time</u>	<u>Priority</u>
P1	0	10	3
P2	1	1	1
P3	2	2	3
P4	3	1	4
P5	4	5	2

- a. Draw four Gantt charts that illustrate the execution of these processes using the following scheduling algorithms: FCFS, SJF, nonpreemptive priority (a smaller priority number implies a higher priority), and RR (quantum = 3). 5%
- b. What is the turnaround time of each process for each of the scheduling algorithms in part a? 5%
- c. What is the waiting time of each process for each of the scheduling algorithms in part a? 5%
- d. Which of the algorithms in part a results in the minimum average waiting time (over all processes)? 5%
9. a. Explain the difference between internal and external fragmentation. 5%
- b. What is the purpose of paging the page tables? 5%