※ 考生請注意：本試題不可使用計算機。　請於答案卷(卡)作答，於本試題紙上作答者，不予計分。

共 8 題，請在答案卷作答一表格如下，並清楚地填入這些題目的答案，否則不予計分。

題號	答案
1	(a)
	(b)
2	
3	
4	請勿在此作答
5	(a)
	(b)
6	(a)
	(b)
	(c)
7	
8	

1. **[20%]** Consider a MIPS processor with an additional floating point unit. Assume functional unit delays in the processor are as follows: memory (2 ns), ALU and adders (2 ns), register file access (1 ns), FPU add (8 ns), FPU multiply (16 ns), and the remaining units (0 ns). Also assume instruction mix as follows: loads (31 %), stores (21 %), R-format instructions (27 %), branches (5 %), jumps (2 %), FP adds and subtracts (7 %), and FP multiplies and divides (7 %).

   (a) What is the delay in nanosecond to execute a load, store, R-format, branch, jump, FP add/subtract, and FP multiply/divide instruction in a single MIPS design?

   (b) What is the averaged delay in nanosecond to execute a load, store, R-format, branch, jump, FP add/subtract, and FP multiply/divide instruction in a multicycle MIPS design?

2. **[15%]** Consider a pipelined processor that executes the MIPS code shown in Figure 1 using the logic of hazard detection and data forwarding unit shown in Figure 2. If the MIPS code cannot be executed correctly, then how do we revise the logic shown in Figure 2 such that the code can be correctly executed?

```
add    $1, $1, $5
add    $1, $1, $6
add    $1, $1, $7
```
Figure 1: The MIPS code

```
if    (MEM/WB.RegWrite
          and (MEM/WB.RegisterRd≠0)
          and (MEM/WB.RegisterRd=ID/EX.RegisterRs))
then ForwardA = 01
if    (MEM/WB.RegWrite
      and (MEM/WB.RegisterRd≠0)
      and (MEM/WB.RegisterRd=ID/EX.RegisterRt))
then ForwardB = 01
```

Figure 2: The logic of hazard detection and data forwarding unit

3. [10%] What is the biased single precision IEEE 754 floating point format of 0.9375? What is the purpose to bias the exponent of the floating point numbers?

4. [5%] Which of the following techniques can resolve control hazards?
   (a) Branch prediction
   (b) Stall
   (c) Delayed branch

5. [15%] In a demand-paging system using a system-wide inverted page table,
   (a) [10%] why are per-process page tables still required?
   (b) [5%] when is a per-process page table accessed?

6. [15%] Which of the following may reduce TLB misses? Explain your answers briefly.
   (a) [5%] increase the level of paging
   (b) [5%] use pre-paging
   (c) [5%] decrease the page size

7. [10%] In Linux, a process cannot hold a spinlock while attempting to acquire a semaphore. Please explain why this policy is in place.

8. [10%] Please explain why UNIX inodes support large files while allowing fast accesses to small files.