編號： 208

國立成功大學 106 學年度碩士班招生考試試題

系　　所：電機資訊學院-資訊聯招

考試科目：計算機組織與系統

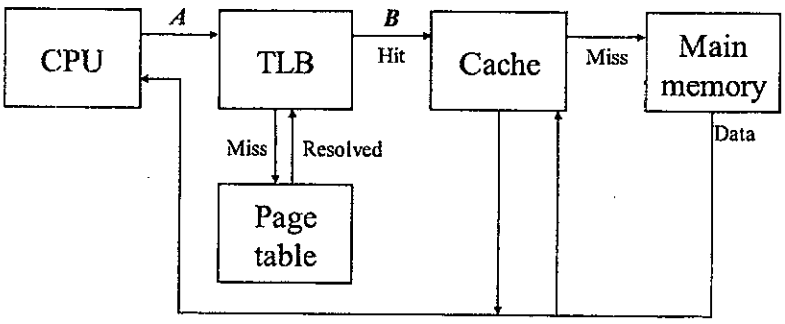
考試日期：0213，節次：1

※ 考生請注意：本試題不可使用計算機。**請於答案卷(卡)作答**，於本試題紙上作答者，不予計分。

共 7 題，請在答案卷作一表格如下，並清楚地填入這些題目的答案，否則不予計分。

題號	答案
1.	(1)
	(2)
	(3)
	(4)
	(5)
	(6)
2.	(1)
	(2)
	(3)
3.	(1)
	(2)
	(3)
4.	
5.	
6.	(1)
	(2)
	(3)
7.	

1. [30%] Consider the following figure.



(1) [5%] What is the name of the TLB's input (Symbol ***A*** in the figure)? (Hint: XXX address.)

(2) [5%] What is the name of the TLB's output (Symbol ***B*** in the figure)?

(3) [5%] What is the name of this type of cache (with ***B*** as its input)? (Hint: XXX cache.)

(4) [5%] Does the **cache aliasing** occur in the cache design shown in the figure (Yes or No)? Explain your answer.

(5) [5%] ``We could have a hit in the cache, and get a TLB miss and a page table miss.'' Is the statement true (Yes or No)? Explain your answer.

(6) [5%] Consider the processor operating at 1GHz. The processor stalls during a cache miss and has the following properties: (i) a cache access time of 2 clock cycles for a hit, (ii) a miss penalty of 100 clock cycles, and (iii) a miss rate of 0.03 misses per instruction. Please compute the **average memory access time**.

2. [10%] Assume the MIPS processor with 5 stages of the pipeline:

(i) IF for the instruction fetch stage,
(ii) ID for the instruction decode/register file read stage,
(iii) EX for the execution stage,
(iv) MEM for the memory access stage, and
(v) WB for the write-back stage.

Given the following instruction sequences.

I1: ADD R1, R2, R0
I2: LW R2, 16 (R1)
I3: LW R1, 4 (R3)
I4: SUB R5, R3, R4

(1) [3%] Find all data dependencies in the instruction sequence.

(2) [3%] Find all hazards in the instruction sequence for the processor **with** and **without forwarding**.

(3) [4%] Sometimes, even with forwarding, we would have to stall one stage for a data hazard. Fortunately, the software technique, Reordering Code, would be adopted to avoid the pipeline stalls. Please state if the instruction sequence suffers from a data hazard that cannot be resolved by the forwarding (Yes or No). If your answer is Yes, please list your reordered code.

3. [10%] Determine whether each of the following statements is True (T) or False (F), and explain your answer.

(1) [3%] Strong scaling is not limited by Amdahl's law.

(2) [3%] Both SMPs and message-passing computers rely on locks for synchronization.

(3) [4%] Multithreading technology in CPUs help reduce the memory latency.

4. [10%] When multiple processes need to cooperate, there is a choice between shared memory and inter-process communication (IPC). Compare and contrast these two techniques. Make sure to clarify the role of the operating system in each.

5. [10%] What is the cause of thrashing? How does the system detect thrashing? Once it detects thrashing, what can the system do to eliminate this problem?

6. [20%] Consider the following snapshot of a system:

	Allocation				Max				Available			
	A	B	C	D	A	B	C	D	A	B	C	D
P1	1	1	2	5	1	7	6	7	2	6	3	1
P2	2	5	4	3	2	9	5	3				
P3	2	4	6	5	2	4	6	7				
P4	2	1	1	1	2	8	6	1				

(1) [5%] What is the content of the matrix Need?

(2) [10%] Is the system in a safe state? Why?

(3) [5%] If a request from process P1 arrives for (1,3,5,1), can the request be granted immediately? Why?

7. [10%] Assume we have a demand-paged memory. The page table is held in registers. It takes 8 milliseconds to service a page fault if an empty page is available or the replaced page is not modified, and 20 milliseconds if the replaced page is modified. Memory access time is 100 nanoseconds.

Assume that the page to be replaced is modified 70 percent of the time. What is the maximum acceptable page fault rate for an effective access time of no more than 200 nanoseconds?