編號： 209

國立成功大學 106 學年度碩士班招生考試試題

系　　所：電機資訊學院-資訊聯招

考試科目：應用電子學

考試日期：0213，節次：2

※ 考生請注意：本試題不可使用計算機。　請於答案卷(卡)作答，於本試題紙上作答者，不予計分。

註：請提供詳細推導過程，並帶入計算數字，不須算出開根號之數字。

1. (20%) Consider the circuit shown in Fig. 1 and the diodes are ideal. (a) Sketch the transfer characteristics (v_o versus v_{in}) (10%). (b) Denote the ON/OFF of diode A and diode B at each segment in (a) (5%). (c) Plot the waveforms of the input and output signals (v_o(t) and v_{in}(t)) (5%).

2. (30%) Consider the circuit in Fig. 2. The NMOS transistor has KP=50uA/V^2, V_{to}=1 V, L=5um, W=500um and $r_d = \infty$. (a) Determine I_{DQ}, V_{DSQ} and g_m (15%). (b) Plot the small-signal equipment circuit for the frequency of v_{in} is in the midband range. (6%). (c) Compute the voltage gain, input resistance and output resistance (9 %).

3. (20%) Consider the circuit shown in Fig. 3. Using the summing-point constraint for both op amps to derive expressions for the voltage gains $A_1 = v_{o1}/v_{in}$ (10%) and $A_2 = v_{o2}/v_{in}$ (10%).

4. (20%) Consider the circuit shown in Fig. 4. Derive an expression for the voltage transfer ratio A(f) (10%). Sketch the magnitude Bode plot to scale (10%).

5. (10%) Design a two-input CMOS NAND gate. (a) Plot the circuit diagram (5%). (b) Show the truth table and ON/OFF of the PMOS and NMOS transistors (5%).

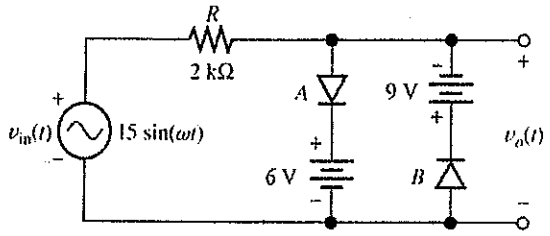

Fig. 1

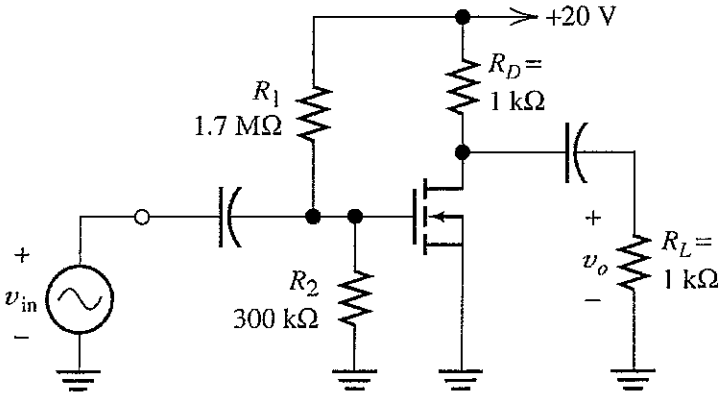

Fig. 2

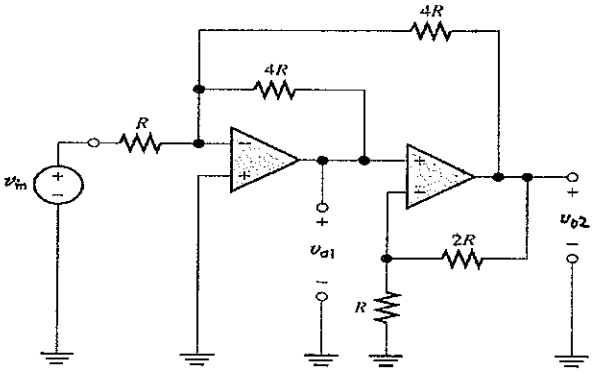

Fig. 3

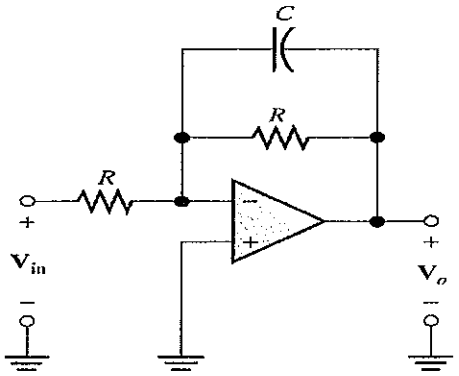

Fig. 4