※ 考生請注意：本試題 □可 ☑不可 使用計算機

1. (15%)

For the circuit shown in Fig.1, evaluate the following (β=100)：

(a) The input differential resistance R_{id}.

(b) The overall differential voltage gain v_o/v_{sig} (neglect the effect of r_o)

(c) The worst-case common-mode gain if the two collector resistances are accurate to within ±1%.

(d)The CMRR, in dB

(e)The input common-mode resistance (assuming that the Early voltage V_A=100V).

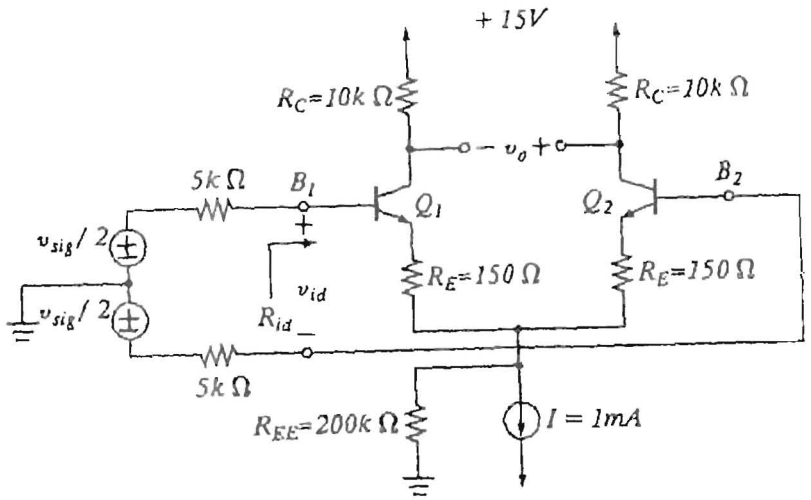

Fig.1

2. (15%)

The network in Fig.2 has $i(t)$= 10cos(50000t) mA. Find the steady-state voltages $v(t)$, $v_L(t)$, and $v_C(t)$.

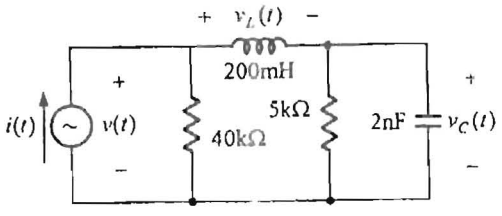

Fig.2

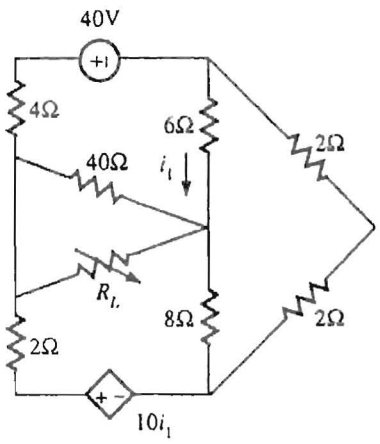

Fig.3

3. (20%)

With the adjustment of the resistor R_L in the circuit of Fig.3, the maximum power delivered to R_L can be achieved. Please calculate the maximum power transferred to R_L?

4. (20%)

A differential to single-ended amplifier is constructed as shown in Fig.4(a). The amplifier

※ 考生請注意：本試題 □可 ☑不可 使用計算機

incorporates Wilson current mirror as active loads. Assuming all of the transistors are in saturation, $\mu_n C_{ox} = 80\mu A/V^2$, $\mu_p C_{ox} = 30\mu A/V^2$, $|V_T| = 0.8V$ for both NMOS and PMOS, $(W/L)_{M1} = (W/L)_{M2} = 320/0.6$, $(W/L)_{M3} = (W/L)_{M4} = (W/L)_{M5} = (W/L)_{M6} = 20/0.9$, $(W/L)_{M7} = 80/0.6$, $(W/L)_{M8} = 160/0.6$. Neglect channel length modulation effect.

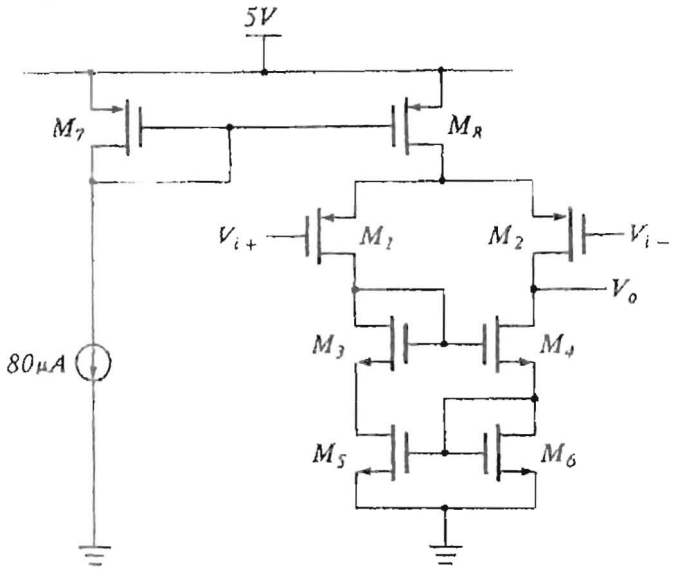

Fig.4(a)

(a) What kind of feedback mechanism is applied in the Wilson current mirror? (shunt-shunt, series-series, shunt - series, series- shunt)

(b) Find out the input common mode ranges $V_{icm(max)}$, $V_{icm(min)}$ of this amplifier.

(c) Consider the circuit shown in Fig.4(b). Assume that $(W/L)_{M3} = (W/L)_{M6} = 21/0.9$, $(W/L)_{M4} = (W/L)_{M5} = 19/0.9$, and the other derives' sizes remain unchanged. If V_i=2.5V, find V_O. (The OP's input offset voltage must be taken into account).

(d) Follow (c) and neglect all the parasitic capacitances of MOSFETs. If V_i is a rising step from 2V to 3V, find the slew rate of V_o. If V_i is a falling step from 3V to 2V, find the slew rate of V_o.

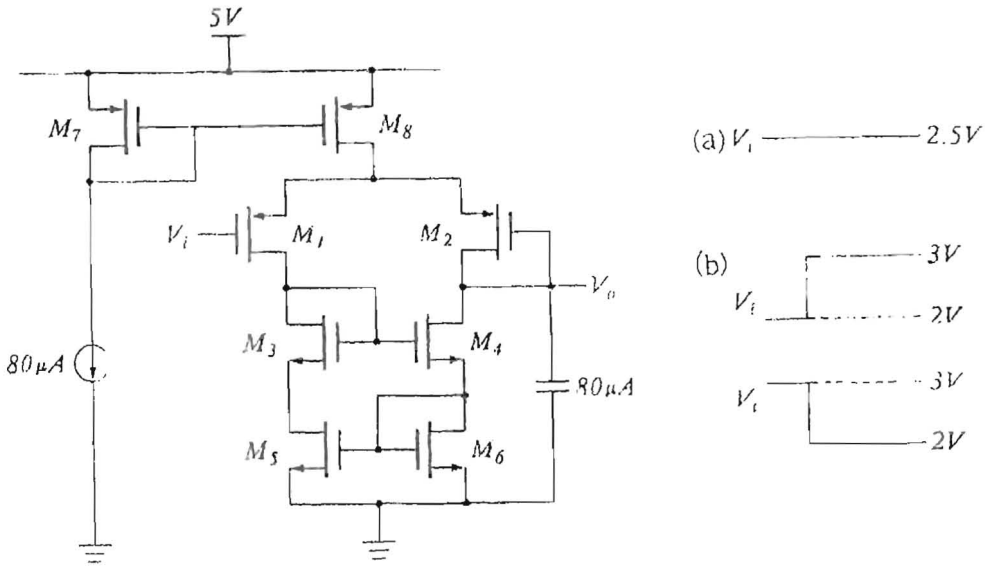

Fig.4(b)

※ 考生請注意：本試題 □可 ☑不可 使用計算機

5. (15%)

Please find the Thévenin and Norton equivalent circuits of the network of Fig.5 at terminals a-b.

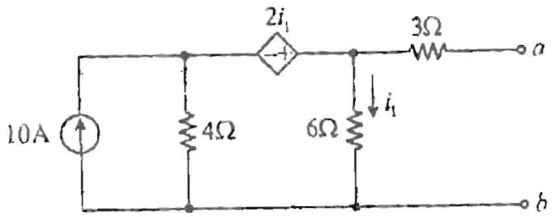

Fig.5

6. (15%)

In the circuit as shown in Fig.6, the junction diode D_1 can be modeled by a forward constant voltage drop of V_r=0.7V；the Zener diode D_2 can be modeled by an ideal Zener voltage of V_Z=3.3V； the op-amp is ideal； the BJT has parameters β=50, $V_{BE(on)}$=0.7V, V_A=∞, $V_{CE(sat)}$=0.5V. The resistors are R_1=R_2=R_3=R_4=R_5=1kΩ, R_6=50Ω. The supply voltage is V_{CC}=12V

(a) Find the voltage V_1 for V_{in}=－10V, －5V, 5V, and 10V.

(b) Derive the expression for V_{out} as function of V_1.

(c) Find the value for R_{in} and R_{out}.

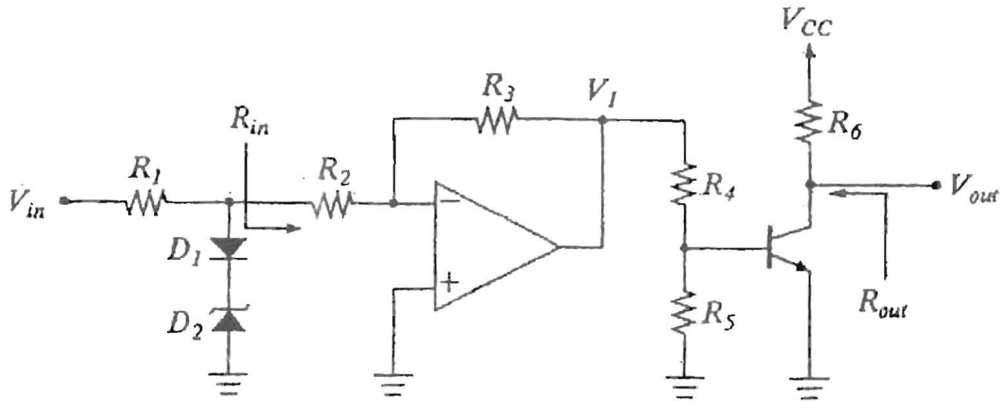

Fig.6