1. 如圖所示之共射極放大器，設 V_{CC}=15V，R_B=200kΩ，R_C=R_E=2kΩ，R_L=6kΩ，Rs=100Ω，V_T=25mV，V_A=100V，β_F=80，試求：(1)I_{CQ} (2)g_m、r_π、r_o、Re (3)R_i (4) R_o (5)A_v。 (20%)

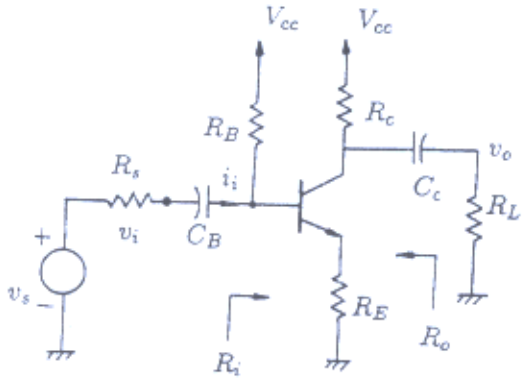

Fig. 1

2. 試求出下圖 a-b 兩點之戴維寧及諾頓等效電路。(20%)

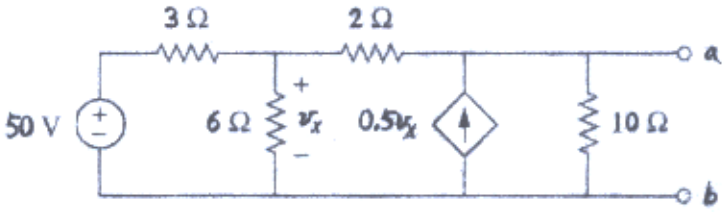

Fig. 2

3. 請說明如圖之 CMOS 所代表的邏輯閘，並列出其真值表。(10%)

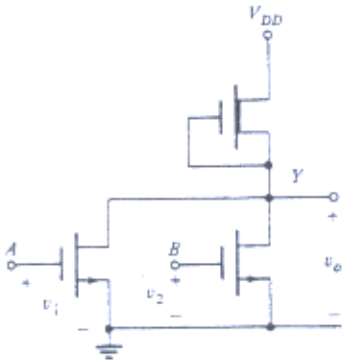

Fig. 3

(背面仍有題目,請繼續作答)

4. 如圖 3.所示，兩個平衡負載連接到方均根 240 千伏 60 赫茲導線，負載 1 有 30kW 與延遲 0.6 的 power factor，負載 2 有 45kWVAR 和延遲 0.8 的 power factor。試求(a)複數、實部與虛部合併負載能量吸收(b) 求傳輸線的電流 (c) 爲了使提升 power factor 至延遲 0.9，求三個Δ相連電容的 kVAR rating 及其電容值。(15%)

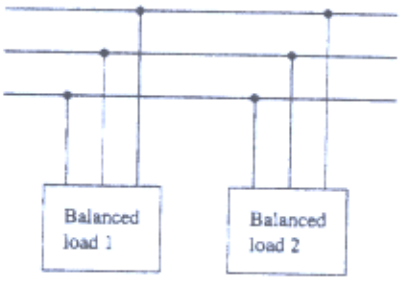

Fig. 3(a)

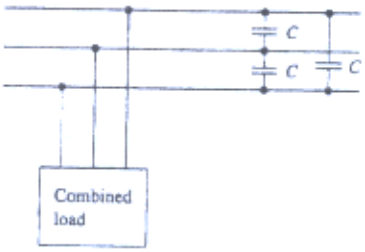

Fig. 3(b)

5. 如圖所示 FET 電路，設 V_{DD}=16V，R_G=1MΩ，R_D=2kΩ，R_s=1kΩ，R_L=10kΩ，且 I_{DQ}=1mA，V_{GSQ}=2V，V_t=1V，k=4mA/V²，V_A=50V，試求：(1) g_m、r_o (2)R_i (3) R_o (4)A_v。 (20%)

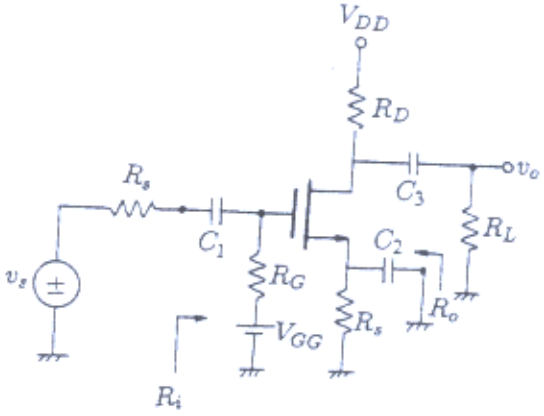

Fig. 5

6. 試求下圖中帶止濾波器之頻寬與中央頻率。(15%)

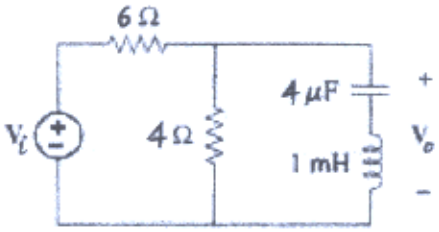

Fig. 6