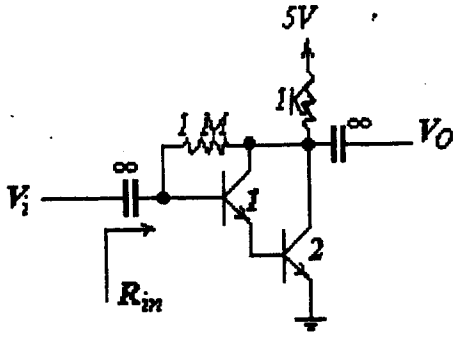
1. **For the circuit shown , the transistor has β=100 and V_{BE} = 0.7 V , find V_o/V_i and R_{in} . (20 %)**



2. **In the following TTL gate (Fig 2) , assume all transistors are identical .**
   $V_{BE(active)}$ = 0.7 V , $V_{BE(saturation)}$ = 0.8 V , $V_{CE(saturation)}$ = 0.1 V , β_F = 100 , β_R = 0.1 , fan-out =1
   (a) Specify which region (forward-active , reverse-active , off , saturation) each transistor is in which V_i is logic "1". (5 %)
   (b) Specify which region each transistor is in which V_i is logic "0". (5 %)
   (c) At the instant when V_i switches from "1" to "0" , specify which region the transistor Q1 and Q6 are in. (10 %)

3. **For the differential amplifier as shown (Fig 3) , β=100 , find : (a) the differential gain , (b) the differential input resistance , (c) the common-mode gain , (d) the common-mode input resistance. (20 %)**

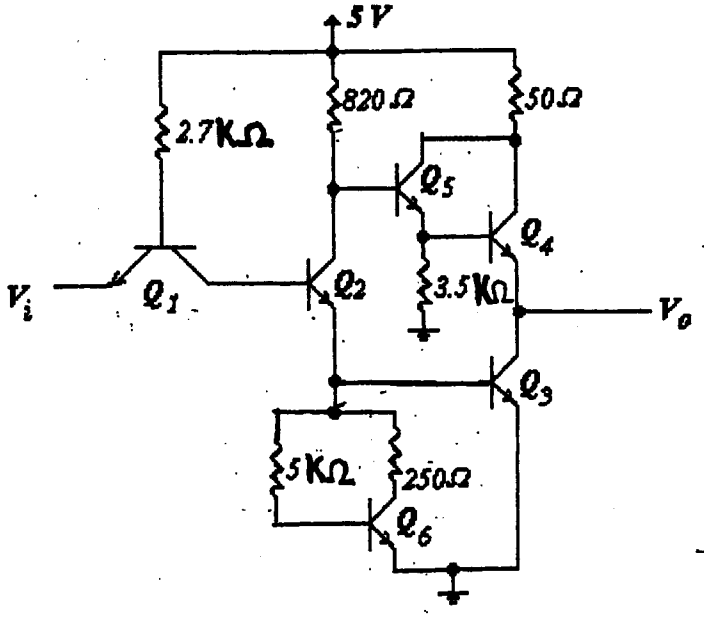


Fig 2

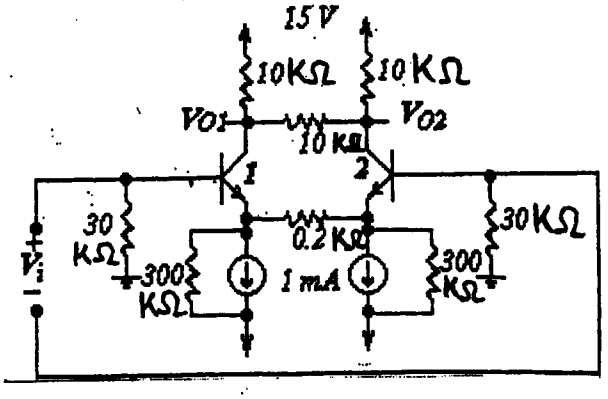


Fig 3

(背面仍有題目,請繼續作答)

4. Consider the network shown in Fig4 . Determine all the load currents. (20 %)

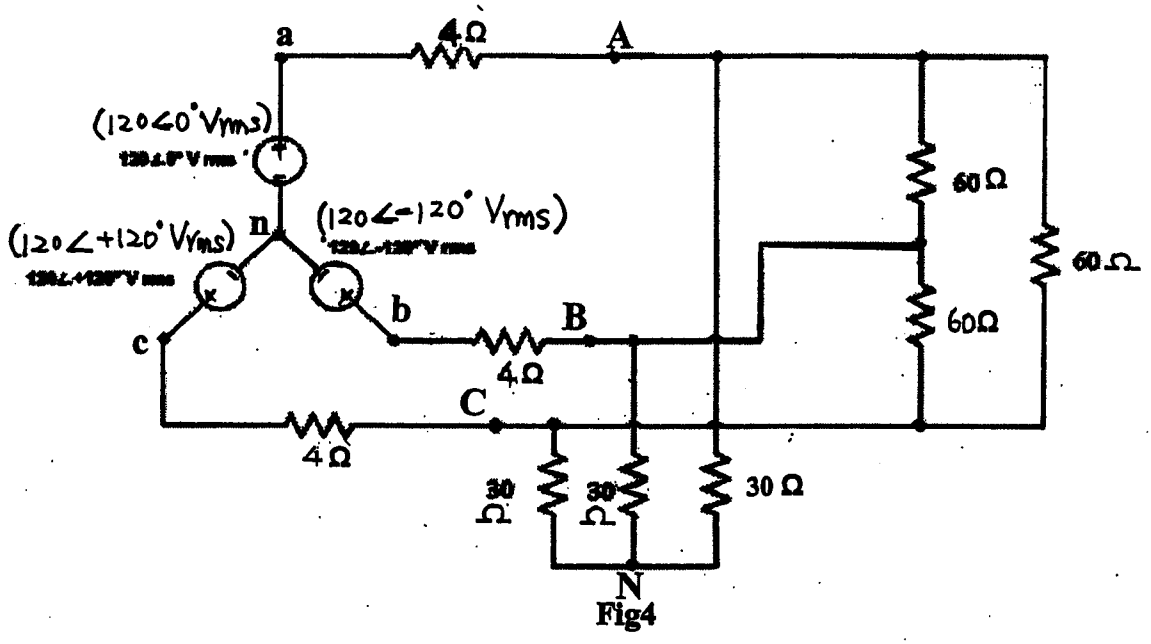


Fig4

5. Find i(t) and v(t) in each of the circuit of Fig5. (10 %)

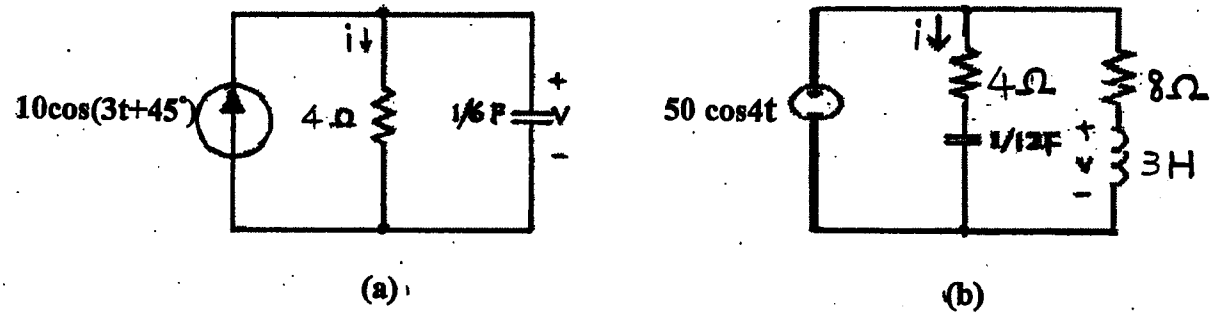


Fig5

6. Derive the Thevenin and equivalent circuits with respect to terminals *a* and *b* of the following circuit (left to a and b) and illustrate it. (10 %)