1. (a) Determine the logic function at the output Y of the circuit shown in Fig. 1A. (10%)
   (b) What is the logic function realized at Y in the NMOS circuit shown in Fig. 1B? (10%)

2. Using the ideal op amp to implement two different non-inverting integrators without inverter. Explain your results in brief. (10%)

3. The op amp in the circuit of Fig. 2 has an open-loop gain of $10^5$ and a single-pole rolloff with $\omega_{3dB} = 10$ rad/s.
   (a) Sketch a Bode plot for the loop gain. (2%)
   (b) Find the frequency at which $|A\beta| = 1$, and find the corresponding phase margin. (4%)
   (c) Find the closed-loop transfer function, including its zero and poles. (4%)

4. Why is Miller-effect compensation often employed to compensate an op amp? (10%)

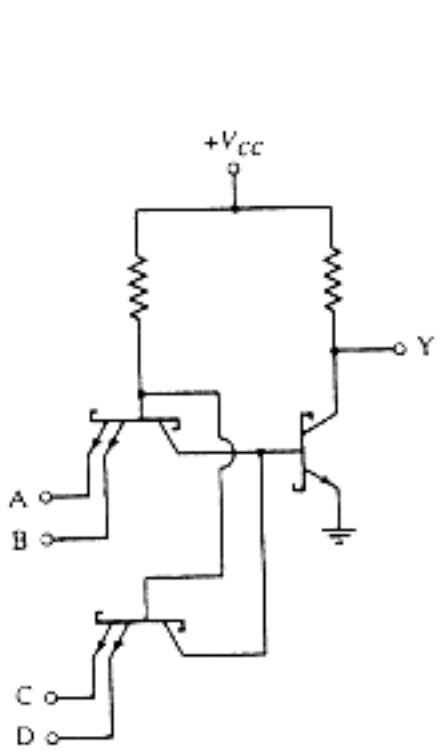


Fig. 1A

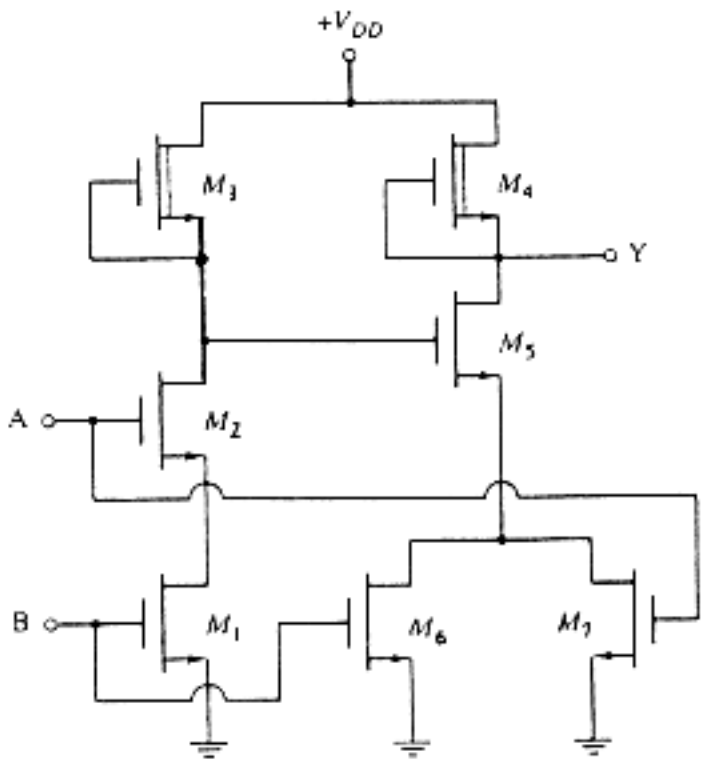


Fig. 1B

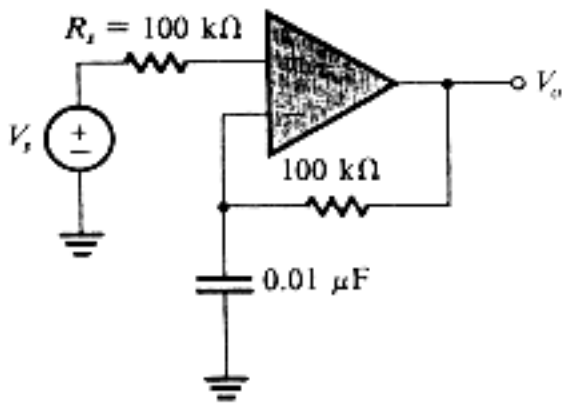


Fig. 2

(背面仍有題目,請繼續作答)

5. Draw the circuit diagram of a 2-bit charge-redistribution A/D converter and explain its operational principle. (10%)

6. The circuit of an amplifier is shown in Fig. 3.
   (a) Express the overall small-signal gain $v_o/v_i$ as a function of $R_S$, $R_C$, $\beta$, $V_A$, and collector current $I_C$. (10%)
   (b) Assume that $R_S = R_C = 50K\Omega$, $\beta = 200$, $V_A = 120V$, determine the value of dc collector bias current $I_C$ that maximizes $v_o/v_i$ (10%).

7. Calculate the bias current $I_{bias}$ of the circuit shown in Fig. 4. Assume that threshold voltage of M1 and M2 is identical, $\mu_n C_{ox} = 20\mu A/V^2$. (10%)

8. Calculate the value of sensitivity $S$ of output current to supply voltage for the circuit of Fig. 5, where $S = (V_{CC}/I_o)(\partial I_o/\partial V_{CC})$. Assume $V_{BE(on)} = 0.7V$. (10%)

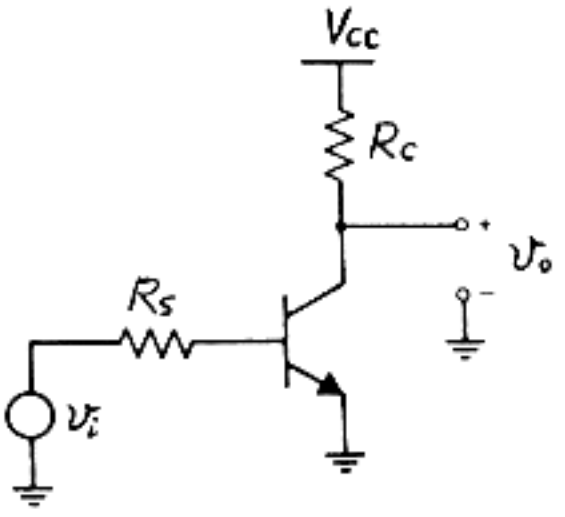


Fig. 3

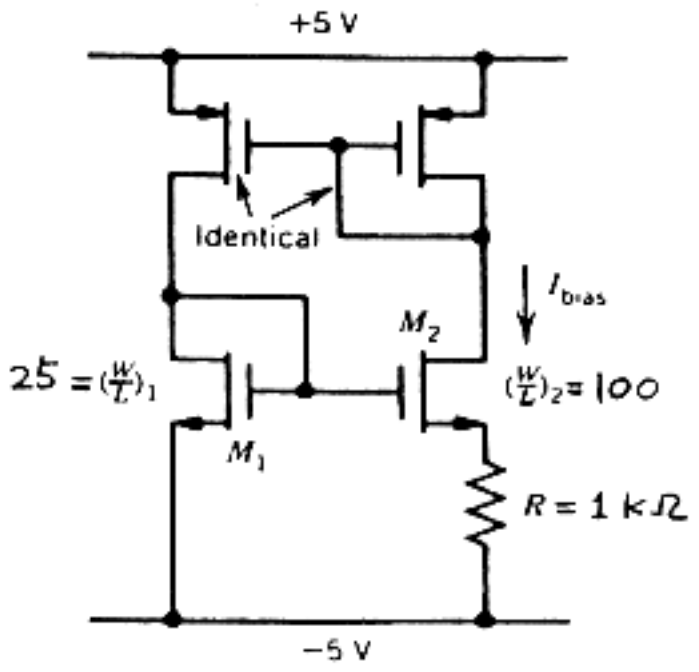


Fig. 4

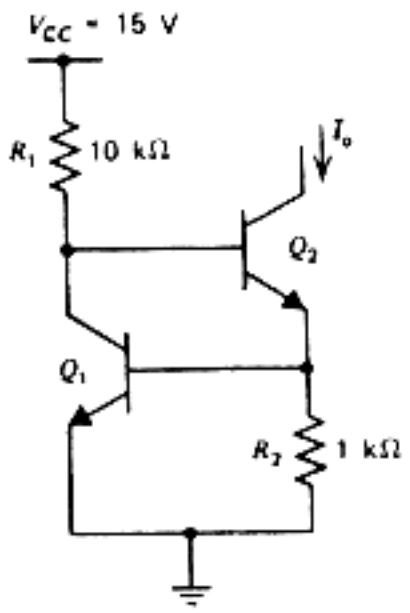


Fig. 5