1. (a)For the source follower in Fig.1 (a), find the open-circuit voltage gain v_{o1}/v_i and the output resistance R_{o1}, in terms of g_{m1} and χ. Neglect the effect of r_{o1} and that of the output resistance of the bias current source. $g_{mb} = \chi\, g_m$, g_{mb} is the body transconductance.

   (b)For the common-gate amplifier in Fig,1(b), find the voltage gain v_o/v_{i2} and the input resistance R_i, in terms of g_{m2}, χ, and R. Neglect the effect of r_{02} and that of the output resistance of the bias current source.

   (c)If the output terminal of the source follower in (a) is connected to the input terminal of common-gate amplifier in (b), find the overall voltage gain v_o/v_i of the cascaded amplifier.

   (d)If V_{DD} = 5 V and the dc bias voltage at the drain of Q_2 is to be 0 V, find the effective voltage ($V_{GS} - Vt$) required for Q_1 and Q_2 so that an overall voltage gain of 25 V/V is realized.

   (e)For I = 50 μA and $k'_n = \mu_n C_{OX} = 50\,\mu A/V^2$, find R and the (W/L) required for Q_1 and Q_2.(15%)

2. As the circuit shown in Fig. 2, design the circuit to obtain a dc gain of 40 dB , a 3-dB frequency of 1.5 KHz., and an input resistance of 1 KΩ. At what frequency does the magnitude of transmission become unity? What is the phase angle at this frequency ? Assume op amp is ideal.(10%)

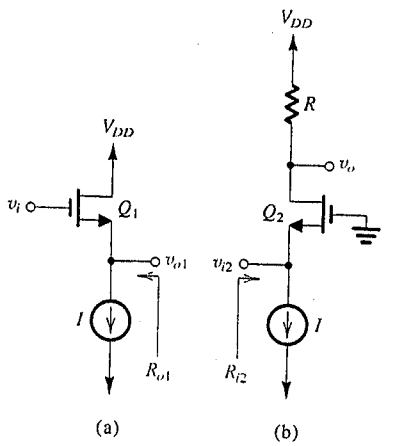


Fig. 1

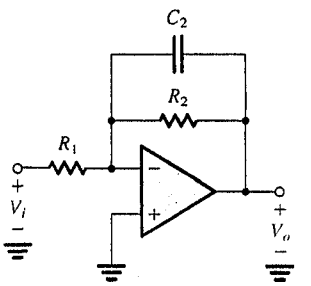


Fig. 2

3. (a)List five characteristics of an amplifier that are modified by negative feedback. (10%)
   (b) Draw the circuit diagram of a switched-capacitor (SC) integrator. (5%)
   (c) Derive the time constant of a SC integrator. (5%)
   (d) Briefly explain why the time constant of a SC circuit can be well controlled. (5%)

4. If the collector current of a BJT operated in forward active region is expressed as
   $i_C = (av_{BE}^2 + bv_{BE})(1 + cv_{CE}) \approx \beta\, i_B$,
   where a, b, c, and β are constant, derive and sketch its small-signal equivalent circuit for the cases of (a) $c = 0$ and (b) $c \neq 0$. (10%)

(背面仍有題目,請繼續作答)

5. (a) Design a MOSFET current mirror to provide currents of I_o and $I_o/2$ simultaneously, where I_o is a constant. (5%)
   (b) Derive the transfer characteristics (i.e., $v_O - v_I$ relation) of the circuit shown in Fig. 3. Assume the Op-Amp is ideal. (5%)
   (c) Draw the load line of the diode D_2 shown in Fig. 4 and find I graphically. Assume D_1 and D_2 are identical diodes, $V_A = 1.5V_\gamma$, where V_γ is the cut-in voltage of the diode. (5%)

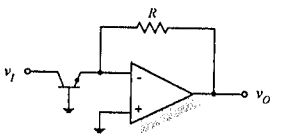


Fig. 3

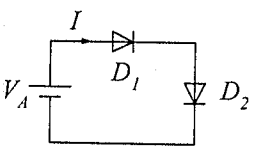
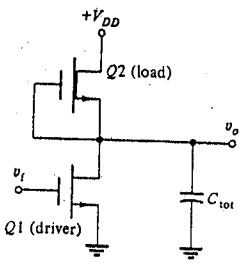
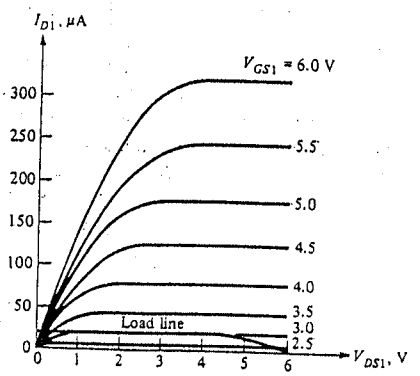


Fig. 4

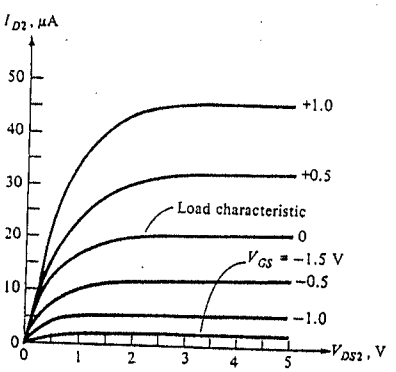
6. An inverter circuit is shown in Fig. a. The output current-voltage characteristics of transistors Q1 and Q2, and the transfer characteristics of this inverter are shown in Fig. b, c, and d, respectively. Assume that C_{tot}=0.3pF and the input signal has V(0)=0.3V and V(1)=6V. Please determine the values of the propagation delay t_{PHL} and t_{PLH}. (25%)



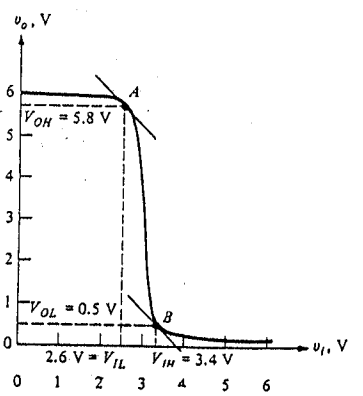
(a)



(b)



(c)



(d)