

1. Calculate the logic low fan-out of the DTL gate shown in Fig .1. (15%)
2. The transistors in the circuit in Fig. 2 both have parameters $V_{TN} = 0.8 \text{ V}$ and $k'_n = 30 \mu\text{A}/\text{V}^2$. (a) If the width-to-length ratios of M_1 and M_2 are $(W/L)_1 = (W/L)_2 = 40$, determine V_O and I_D . (b) Repeat part (a) if the width-to-length ratios are changed to $(W/L)_1 = 40$ and $(W/L)_2 = 15$. (18%)
3. Your answers must be as brief as possible for the following questions
 - (a) Draw a block diagram of a two-stage OP-AMP, and briefly explain the function of each block. (3%)
 - (b) What are the advantages of using active loads in OP-AMP IC design? (3%)
 - (c) Define a (I) class A, (II) class B, and (III) class AB amplifier. (3%)
 - (d) List three advantages of class B over class A. (3%)
 - (e) What are the characteristics of an amplifier that can be modified by negative feedback? (3%)

4. Suppose you have an amplifier with a transfer function given by

$$a(j\omega) = \frac{10^5}{(1 + j\omega/10^3)(1 + j\omega/10^5)(1 + j\omega/10^6)}$$

and you apply negative feedback to the amplifier, using a feedback network that is not a function of frequency. If you desire to have a closed-loop gain of 30 dB with a 45° phase margin (PM), and you compensate the loop by moving the dominant pole frequency down, what new pole frequency should be used? (10%)

5. For the circuit in Fig. 3.
 - (a) Find the loop gain $L(s)$, and the oscillation frequency f_0 . (6%)
 - (b) The ratio of R_2/R_1 for oscillation. (4%)
6. For the diode circuit shown in Fig. 4, write the load line equation and draw the possible load line for the diode using (a) a constant resistor or (b) a depletion-mode n-MOSFET with $V_{GS} = 0 \text{ V}$ or (c) an enhancement-mode n-MOSFET with $V_{GS} = V_{DS}$ as the load device. (15%)
7. For the circuit in Fig. 5(a) and the corresponding i - v characteristics in Fig. 5(b), if the dc operation point of the MOSFET is set at $(I_{DQ}, V_{GSQ}) = (1.5 \text{ mA}, 3.5 \text{ V})$, find the value of V_{DD} , R_D , R_{G2} , and voltage gain $A_v (= dv_o / dv_i)$. Assume threshold voltage $V_t = 1 \text{ V}$ and $R_{G1} = 100 \text{ M}\Omega$. (17%)

(背面仍有題目，請繼續作答)

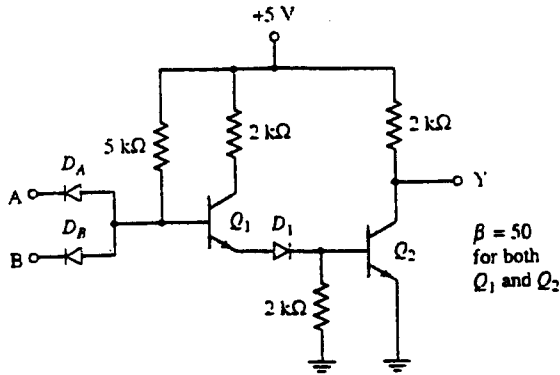


Fig. 1

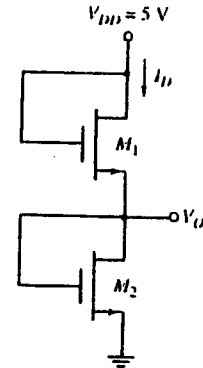


Fig. 2

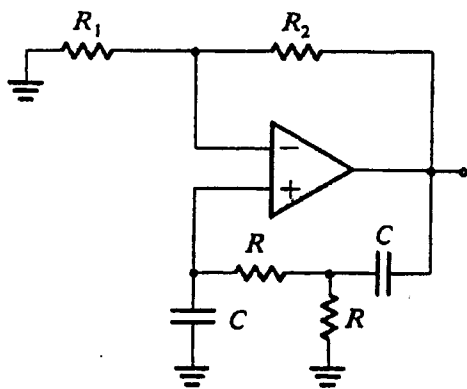


Fig. 3

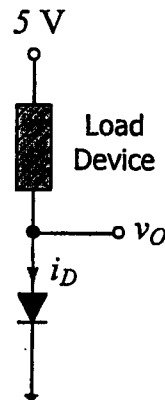


Fig. 4

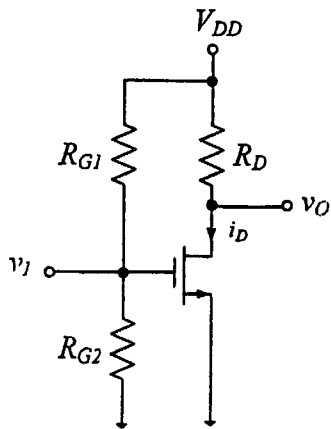


Fig. 5(a)

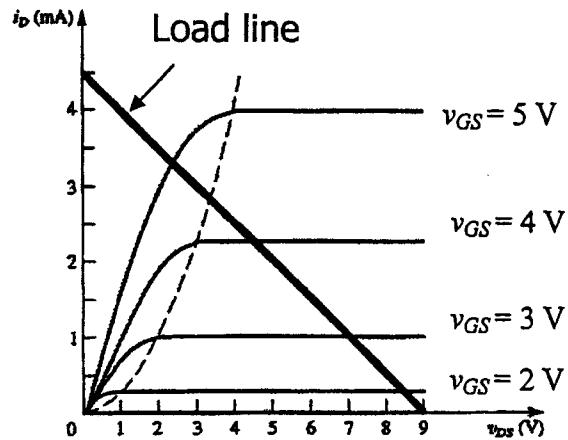


Fig. 5(b)