本試題是否可以使用計算機：☑可使用 ，☐不可使用 （請命題老師勾選）

1. The characteristics for transistors Q_1 and Q_2, used in the circuit shown in Fig. 1, are given in Figs. 2 and 3, respectively. Determine V_{DS1} and V_{DS2}. (13%)

2. A TTL NAND gate with a totem-pole output is shown in Fig. 4. If all transistors are identical and the related parameters of transistor and diode are: $V_{BE(cut\text{-}in)}$=0.5V, $V_{BE(on)}$=0.7V, $V_{BE(sat)}$=0.8V, $V_{CE(sat)}$=0.2V, $V_{DO(cut\text{-}in)}$=0.6V, $V_{DO(on)}$=0.7V. Please determine the average static power dissipation $P_{(av)}$ and dynamic power dissipation $P_{(dyn)}$ of this gate. (20%)

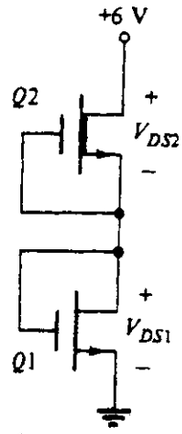

Fig. 1

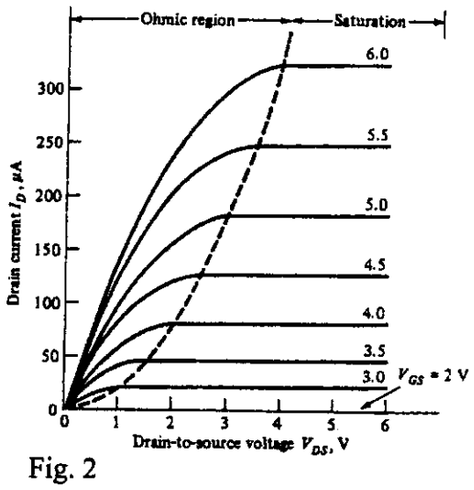

Fig. 2

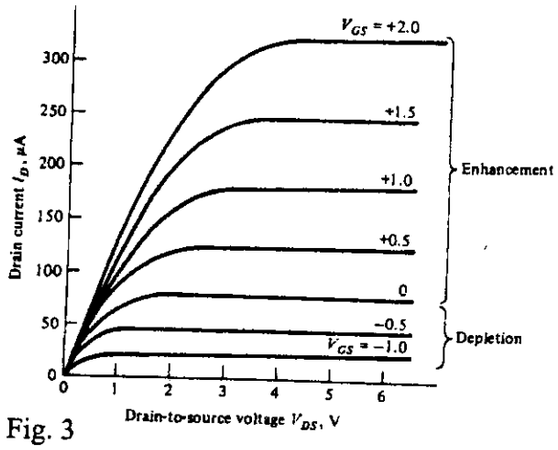

Fig. 3

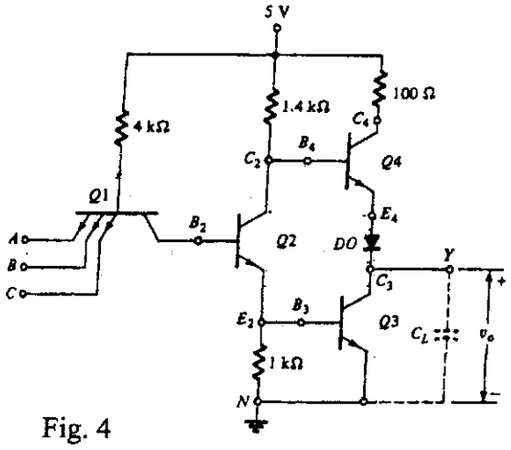

Fig. 4

3. Please answer briefly for the following questions.

(a) For class A, B, and AB amplifiers, which one has the maximum possible power conversion efficiency? Explain the condition that the maximum efficiency can be

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obtained in the amplifier. (3%)

(b) List the four basic feedback topologies for amplifiers, which topology is desirable for the design of a current amplifier. (3%)

(c) What is the function of CC in the CMOS op-amp circuit as shown in the attached Fig. 5? (3%)

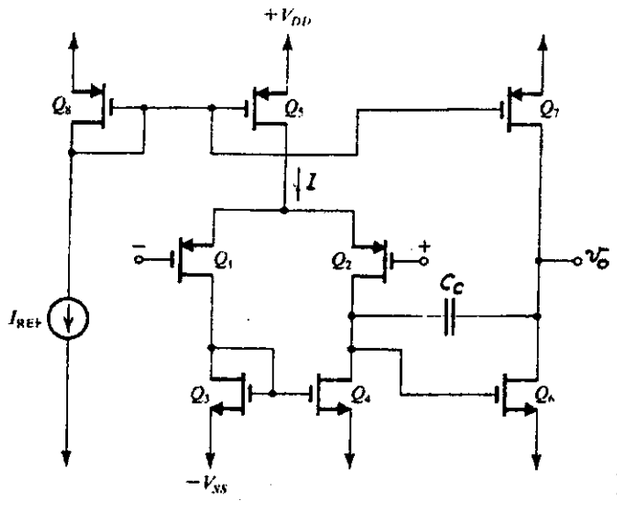

Fig. 5

4. Use the feedback method to analyze the circuit shown in the Fig. 6, Find

(a) what is the feedback configuration of this circuit? (3%)

(b) the feedback factor β and the voltage gain vo/vs (6%)

(c) the input resistance Rin and the output resistance Rout. (6%)

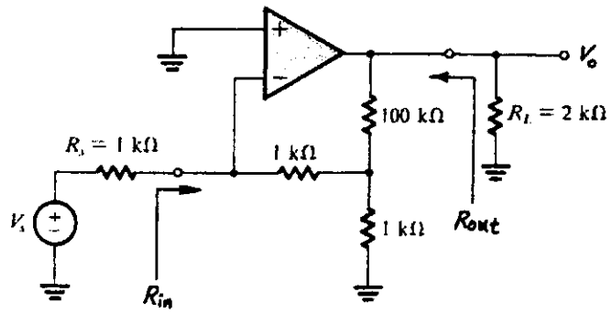

Fig. 6

The op-amp has open-loop gain μ = 104 v/v, Rid = 100 kΩ, ro = 1 kΩ.

5. For the circuit shown in Fig. 7, assume the diode voltage drop is 0.7V.

(a) Show the analysis of this circuit that the oscillation can be obtained. (5%)

(b) Find the frequency of oscillation, and the amplitude of the output sine wave in peak-to-peak value. (5%)

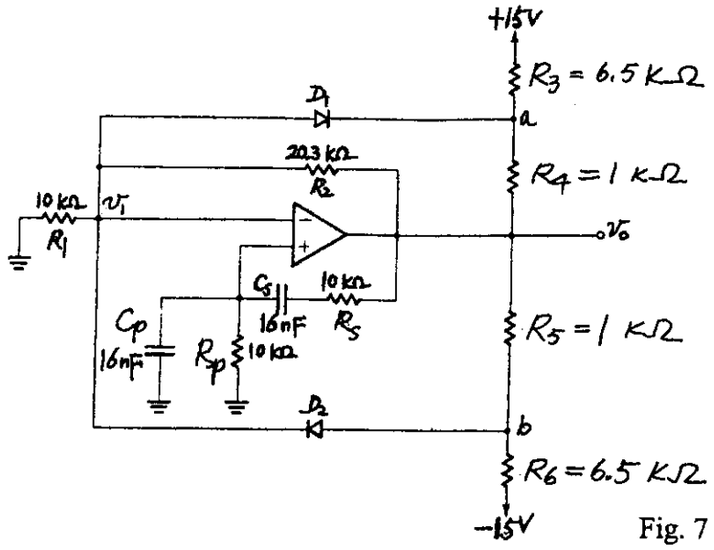

Fig. 7

6. Please answer or explain briefly the following questions.
   (a) The reason why transistors could act as transfer resistances. (5%)
   (b) The bias condition for a transistor to operate as a linear amplifier. (5%)
   (c) For a CMOS inverter with matched MOSFETs having threshold voltage V_t=1 V, find the noise margin if V_{DD}=5 V. (5%)
   (d) What is the small-signal resistance of a diode biased to operate at a dc current I_D. (Assume the diode follows $i_D = I_o(\exp(\frac{v_D}{V_T}) - 1)$.) (5%)

7. (a) Draw the load line of D_2 for the circuit shown in Fig. 8. Assume that D_1 and D_2 are matched diodes and V_A=4V_γ, where V_γ is the cut-in voltage of the diode. (10%)
   (b) State one of the possible methods to double the current I? (3%)

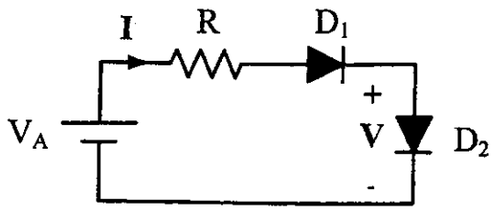

Fig. 8