## 資訊工程研究所

PART I

6% ① 分別說明 cpu 進入 ① Fetch cycle ② Execution cycle ③ Interrupt cycle 時所執行的工作（operations）

4% ② 為什麼 I/O interfaces 常需要配備一個或一個以上的 Data Buffer 來傳送（transmit）或接收（Receive）Data？請以 serial I/O interface 為例說明之。

8% ③ 為一個具有 single bus organization 的 cpu 設計它的 General Purpose register 的線路，請以一個 bit 為例畫出其詳細線路圖。

6% ④ 說明 Subroutine 和 Interrupt Service Routine 的異同處

6% ⑤ 在 common bus 的 Multiprocessor System 中為什麼每個 processor 需要有 bus Lock 的能力？請舉例說明之

12% ⑥ 比較下列各組名詞的差異

① Half duplex, Full duplex

② Asynchronous Transmission, Synchronous Transmission

③ tightly coupling, Loosely coupling

④ Hardwired control, Microprogrammed control.

3% ⑦ 考慮具有二種 state 的 cpu，請舉出 5 個不同的 privileged instructions

5% ⑧ 請舉二種 cpu 與 I/O 之間的同步方法，並說明之。

PART II.

1. A binary multiplier that multiplies two 4-bit numbers $m_3m_2m_1m_0$ and $q_3q_2q_1q_0$.
   (a) Use logic circuit to implement this array multiplier. Find the ouput functions and draw the logic circuit diagram. (8%)
   (b) Use a ROM to implement this multiplier, and explain your circuit including the ROM content in detail. (8%)
2. Design a synchronous 2-4-2-1 BCD count-up counter using JK flip-flop. (use A,B,C,D as the FF's name)
   (a) Obtain the excitation table of this counter. (4%)
   (b) Derive the flip-flop input functions of this counter. (12%)
   (c) Draw the logic circuit of (b). (2%)
3. Using JK flip-flop to design a typical stage of an accumulator that performs the following microoperations: (16%)

| | | |
|---|---|---|
| $P_1$: | A<-A+B | Add B to A |
| $P_2$: | A<-0 | Clear A |
| $P_3$: | A<-A/ | Complement A |
| $P_4$: | A<-A^B | And B to A |
| $P_5$: | A<-AvB | OR B to A |
| $P_6$: | A<-A+B | Exclusive-OR B to A. |