PART I:

計算機結構

1. 解釋名詞:
   (1) memory-mapped I/O (2%)
   (2) pipeline processing (2%)
   (3) relative-addressing mode (2%)
   (4) RISC (1%)
   (5) systolic array processor (2%)
   (6) shuffle-exchange network (1%)

2. (1) 何謂 cache memory? (2%)
   (2) 舉出三種 main memory 至 cache memory data transformation 的 mapping types。(4%)

3. 試列舉四種 CPU 與 peripheral devices 間傳送資料 (data transfer) 的方式,並舉例說明之。(6%)

4. (1) 何謂 daisy chain priority interrupt? (2%)
   (2) 試繪出含有三個 devices 及一個 CPU 的 daisy chain priority interrupt 系統結構圖,並詳述其中一個 stage 的 priority arrangement 電路。(4%)

5. 比較 control-driven computers, data-driven computers 及 demand-driven computers 之異同。(4%)

6. 試說明設計 firmware program 及 software program 的差異。(4%)

7. 試說明 future generation computer systems 應有的特性。(4%)

8. 試於 IBM PC 上設計一個 intelligent printer I/O card,使能
   (1) 同時控制一台具 centronic interface 及一台具 RS-232C interface 的 printers 印製檔案,
   (2) 重覆印製同一檔案多次,而僅需接受來自 host 的 command 一次,
   (3) 在 printers 尚未完成印製工作時,host 能執行其它工作 (如利用 PE-II 編輯另一檔案),
   繪出 block diagram,並說明各 block 的机能與動作。(5%)

9. 設有一個 computing problem，若在 uniprocessor 執行需一單位時間($T_1=1$)；現利用一套 n-processor parallel computer 計算同一問題，而且
(1) 對 n 個可能的 operating modes (在 n-processor system 中，可能同時指定其中 i 個 processors 執行運算，$i=1,2,\cdots,n$) 選擇機率相同，即 $f_i=1/n$，
(2) 對任一 operating mode，其每個 working processor 的工作量相同，即 $d_i=1/i$，

試証明此一 n-processor parallel computer 的 speedup 上限 (upper bound) 為 $n/\ln n$. (5%)

PART II:

Digital Design

1.
(a) Describe the procedure for the subtraction with (r-1)'s complement. Assume the minuend M and the subtrahend N are in base r and both are positive. (4%)
(b) Prove the above procedure. (5%)

2. Using exclusive-OR (or equivalence) gates to design a combinational circuit which checks for even parity of four bits (Don't use other kinds of gates). (8%)

3. Design a counter that counts the decimal digitals according to the 2,4,2,1. Use T flip-flops. (10%)

4.
(a) Implementing a full-adder with two half-adders and an OR gate. (3%)
(b) Design a 4 bits full-adders with look-ahead carry and compute the total delay time in this adder. (8%)

5. A digital system has three registers: AR, BR, and PR. Three flip-flops provide the control functions for the system: S is a flip-flop which is enabled by an external signal to start the system's operation; F and R are used for sequencing the micro-operations. A fourth flip-flop, D, is set by the digital system when the operation is completed. The function of the system is described by the following register transfer operation:

S: PR <- 0, S <- 0, D <- 0, F <- 1
F: F <- 0, if (AR=0) then (D <- 1), if (AR <> 0) then (R <-1)
R: PR <- PR+BR, AR <- AR-1, R <-0, F <- 1

(a) Show that the digital system multiplies the contents of AR and BR and places the product in PR.
(b) Draw a block diagram of the hardware implementation. Include a start input to set flip-flop S and a done output from flip-flop D. (12%)