國立成功大學 79 學年度資訊工程研究所考試(計算機概論試題)

PART I. LOGIC DESIGN.

1. Design an 8421 BCD adder/subtractor with a control input to select between the addition and subtractions.
   - (a) Use logic circuit.   (7%)
   - (b) Use a ROM.   (3%)

2. (a) Reduce the number of states in the following state table and tabulate the reduced state table.   (5%)

Present state	Next state		Output	
	$x = 0$	$x = 1$	$x = 0$	$x = 1$
a	f	b	0	0
b	d	c	0	0
c	f	e	0	0
d	g	a	1	0
e	d	c	0	0
f	f	b	1	1
g	g	h	0	1
h	g	a	1	0

(b) If the binary assignment of the reduced state table of (a) is assigned as (001, 010, 011, 100, 101, ...) from state a in order. Design the sequential circuit with three JK flip—flop. (Use A, B, C, as the FF's name). (15%)

3. A multiplier which uses the standard add and shift algorithm (fig. 1) is shown in fig. 2, the MQ—register holds the multiplier and the MPCND—register holds the multiplicand, Z_1, Z_2, Z_3, Z_4 are the control signal of control circuit.
   - (a) Draw the ASM (Algorithm State Machine) chart of the control circuit of this multiplier.   (5%)
   - (b) Derive the state table for the ASM chart of (a).   (5%)
   - (c) Design the control circuit with D flip—flop and a decoder. (5%)
   - (d) Draw the equivalent state diagram and design the circuit with one flip—flop per state.   (5%)

```
BEGIN Multiplication
    WAIT UNTIL start
    AC: = 0; E: = 0;
    REPEAT 32 times
    BEGIN
        IF MQ[32] = 1 THEN E AC: = AC + MPCND;
        RIGHTSHIFT(E AC MQ);
    END
    Completion: = 1
END Multiplication
```
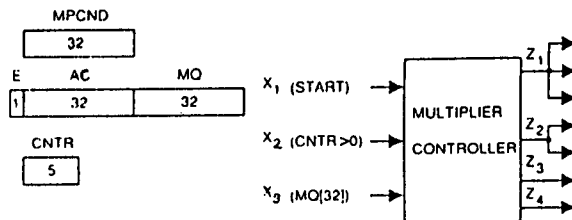
Fig. 1

Fig. 2

PART II.

1. 何謂 Nanoprogrammed Computer. 並說明它的優缺点。(7%)

2. 在設計 Control unit 時有所謂的 delay-element method 之設計法. 舉例說明之.
(7%)

3. 試述降低 pipelined computer 中 reinitiation (resynchronization) rate 的方法。(7%)

4. 說出至少四種增加 cpu-memory interface bandwidth 之方法。(7%)

5. Bus Arbitration 之設計方式有那幾種? 說明之。(7%)

6. 解譯名詞: (15%)
   ① RISC   ② Silicon Compiler   ③ data coherence   ④ data dependency
   ⑤ Reentrant   ⑥ SIMD   ⑦ latency   ⑧ starvation   ⑨ ASIC
   ⑩ Associated Memory.