1. **Computer Organization [40%]**

We are designing the memory system of a router that is to be used for the gateway of a dedicated communication network. The routing table for the router consists of 64 Mbytes and is organized in 1024-byte table entries. To achieve the desired performance it is essential to have the whole routing table resident in the main memory. The routing program (that uses the routing table to determine how to route the packets) is 2 Mbytes. The CPU used for the system generates 32 bit real addresses. To achieve the desired performance, it is also considered necessary to use a cache which is to be 8 Mbytes and has to be organized using a block size of 256 bytes. The cycle time of the main memory is 1 *u*sec and that of the cache is 50 *n*sec.

a) How large a main memory you would put in the system and why?
b) Give a detailed organization of the cache scheme you will use. Clearly identify all components of the address fields and how they are to be used.
c) What cache mapping scheme you would use and why?
d) What information will have to be kept with each block of cache and how will this information be organized.
e) What cache replacement policy would you implement and why?
f) How would you handle the update of routing table entries?

2. **Operating Systems [20%]**

A paged virtual memory scheme provided each process with four virtual memory segments, each with a maximum size of 1 Mbytes (2^{20} bytes).
This scheme is to be implemented on an architecture that supports a maximum physical memory size of 32 Mbytes (2^{25} bytes). The architecture provides a single base register (the content of which is part of the state of a process) from which to start the virtual address translation process. Pages of size 4 Kbytes are to be used.

a) Design a virtual address translation mechanism that implements the above scheme on this architecture. Your design should consist of **drawing** a diagram that describes the translation process, along with a brief **written description** of how the translation occurs. For any translation tables you use in the design, please indicate the maximum length (number of entries) of the table, along with an estimate of its width (number of bits needed per table entry). Indicate how you get these numbers.

3. Compilers [20%]

a) What are *call by value*, *call by reference*, and *call by copy-and-restore* ? Please give an illustrative example of each.

(背面仍有題目,請繼續作答)

b) What is dynamic linking?

c) Why do we need dynamic linking (or what will happen if we do not have dynamic linking)?

d) Describe a mechanism in which the compiler and the operating system work together to support dynamic linking.

4. **Computer Networks[20%]**

A well-known medium access control (MAC) protocol is CSMA/CD. The basic behavior of the CSMA/CD can be described as follow.

1.If the medium is busy, then wait until the medium is free.

2.If the medium is free, then transmit data.

2.1 If the transmission collides with others, then wait for a random number of time units

2.2 Go back to step 1.

CSMA/CD stands for Carrier Sense Multiple Access / Collision Detection.

a) Please indicate which step in the above description does the "carrier sense" part, and which step does the "collision detection" part of the protocol.

b) Consider the following scenario in which sender C is transmitting the data from time 0 to time 3. Sender A wants to transmit data and starts its CSMA/CD protocol at time 1, and sender B starts at time 2. Is it true that senders A and B will collide at least once before either of them starts the transmission? If yes, when does it (i.e. the collision) happen? Drawing a time chart will help the grading.

c) Continue on b), please rewrite the protocol to try to avoid such a collision.