1. True/False questions. Give your reasons if it is *false*.

[25%; gain 5 points for each correct answer and drop 1 point for each wrong answer]

(a) Looping is one reason to cause *spatial locality*.

(b) Input / Output completion interrupt is *asynchronous* interrupt.

(c) The advantage of paging over segmentation is that paging uses *physical concept*.

(d) 6-stage Johnson counter is modulus of 12.

(e) *LS TTL* family has higher noise margin than *CMOS* family.

2. Operating Systems [25%]

Briefly explain the following terms:

(a) dynamic address translation

(b) swap time

(c) loosely coupled multiprocessing system

(d) round robin scheduling

(e) preemptive

3. Computer Organization [25%]

Suppose a computer's address size is k bits (using byte addressing), the cache size is S bytes, the block size is B bytes, and the cache is A-way set-associative. Assume that B is a power of two, i.e. $B = 2^b$. Estimate the following quantities in terms of S, B, A, b, and k.

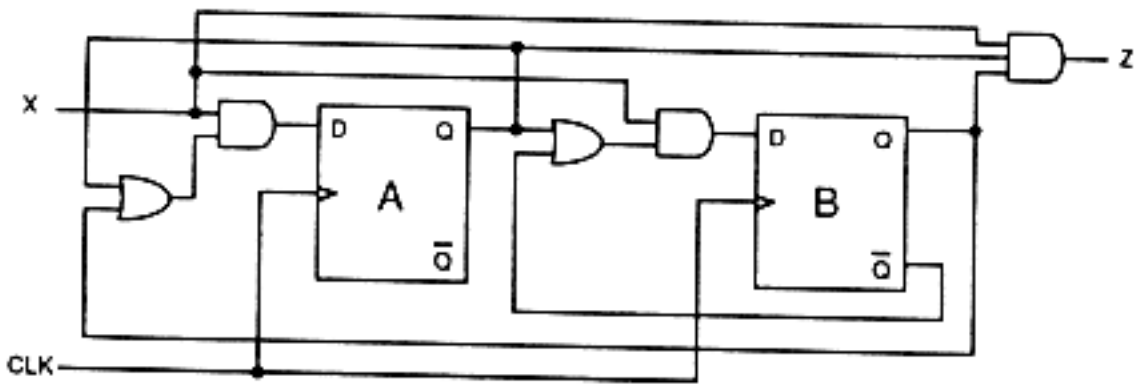
(a) the number of sets in the cache

(b) the number of index bits in the address

(c) the number of bits needed to implement the cache

4. Logic Design [25%]

In the following block diagram of a sequential logic circuit;



(a) write down *state table*

(b) draw *state diagram*

(c) explain the function of the circuit and illustrate the working process in detail