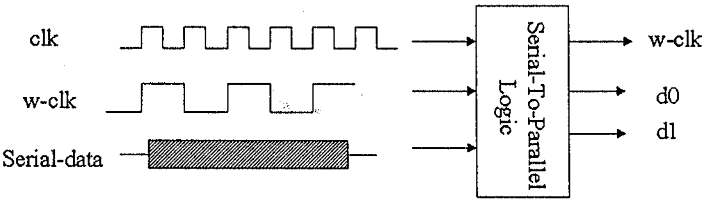
90 學年度 國立成功大學 碩士班招生考試 資訊工程 系所 計算机組織/系統 試題 共 2 頁 第 1 頁

1. **Logic Design:** (25%) Design a Serial-To-Parallel receiver (2-bit) based on the three input signals shown in the following diagrams. You can use logic gates and Flip-Flops as your basic building elements.



2. **Computer Organization:** (25%) For a pipeline processor, there are 3 clock cycles of latency for multiplication operations, there are 2 clock cycles of latency for any other ALU operations and there is 1 clock cycle of latency for any Branch operations and Load/Store operations. Let **AR0** be an auxiliary register and **R0, R1,** and **R2** be data registers. For the following C codes,

```
for (i=1;i<=256;i++){
    a+=f(i)*g(i); }.
```

Let the associate assembly codes be as follows.

```
Loop:   LOAD   R0, 0(AR0)       ;  R0 = *(AR0)
        LOAD   R1,1024(AR0)     ;  R1 = *(AR0+1024)
        MPY    R0,R0,R1         ;  R0 = R0 * R1
        ADD    R2,R2,R0         ;  R2 = R2 + R0
        SUB    AR0,AR0,#1       ;  AR0 = AR0 – 1
        JNZ    AR0, Loop        ;  Jump to Loop if AR0=0
```

Initial conditions for registers and data arrangement are set such that they are suitable for the execution of the corresponding C codes.

(a) (8%) How stalls are inserted into the above program if no scheduling is performed? How many clock cycles are required for the job?

(b) (12%) Reschedule the above program such that the least number of clock cycles is required for the job.

(c) (5%) Find the number of clock cycles required based on your design in (b).

(背面仍有題目,請繼續作答)

3. **Operating System.** (25%)
   - (a) (5%) Please indicate a technique to separate the user logical memory and the physical memory. Please propose one method used to implement this technique and explain how it works briefly.
   - (b) (5%) Please indicate a technique that can reduce the traffic between a main memory system (such as a disk or DRAM) and a CPU by using fast memory device. Please propose one method to implement this technique and explain how it works briefly.
   - (c) (5%) Explain the relation between your answers in (a) and (b).
   - (d) (5%) Both the techniques in (a) and (b) suffer from a similar phenomenon. Explain it. How to handle this problem.
   - (e) (5%) How to evaluate the performances of your answers in (a) and (b).

4. **Compiler.** (25%) Answer the following questions.
   - (a) (5%) (True/False) The LR(1) parsing table for a grammar has a shift/reduce conflict if and only if its LALR parsing table has one.
   - (b) (5%) (True/False) For every context-free grammar, its LALR parsing table and its LR(0) parsing table have exactly the same number of states.
   - (c) (5%) (True/False) If a grammar produces a shift/reduce conflict when run through YACC (using no precedence rules) then it is necessarily ambiguous.
   - (d) (5%) (Select one answer that is correct.) For the compilation of a C program, activation record is generally happened or generated at (a) lexical analysis phase (b) syntax analysis phase (c) semantics analysis phase (d) code generation phase (e) none of the above.
   - (e) (5%) (Select one answer that is the best.) Suppose in a C program there is a variable that is declared but never used in the program. For such a situation the compiler usually gives a warning to the programmer. To detect such a situation in the process of compilation, which compilation phase(s) of a compiler you think can be coded to achieve such a capability? (a) syntax analysis phase only (b) semantic analysis phase only (c) code optimization phase only (d) symbol-table management phase only (e) code optimization phase or symbol-table management phase (f) lexical analysis phase, semantic analysis phase or symbol-table management phase.