系所組別：光電科學與工程學系乙組

考試科目：電子學　　　　　　　　　　　　　　　　　　　　　考試日期：0223，節次：1

※ 考生請注意：本試題不可使用計算機。　請於答案卷(卡)作答，於本試題紙上作答者，不予計分。

1. The op amplifier, shown as Fig.1, is ideal with output saturation levels of ±12 V. Assume that when conducting the diode exhibits a constant voltage drop of 0.7 V. (a)Please find V_A, V_0 and V_- for V_I=+1V (6%)(b) Please find V_A, V_0 and V_- for V_I=-1V (6%) (c) find the **average output voltage** obtained when V_I is a symmetrical square wave of 1-kHz frequency, 5-V amplitude and zero average. (3%)
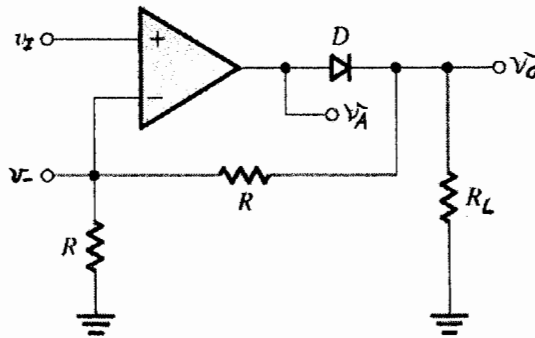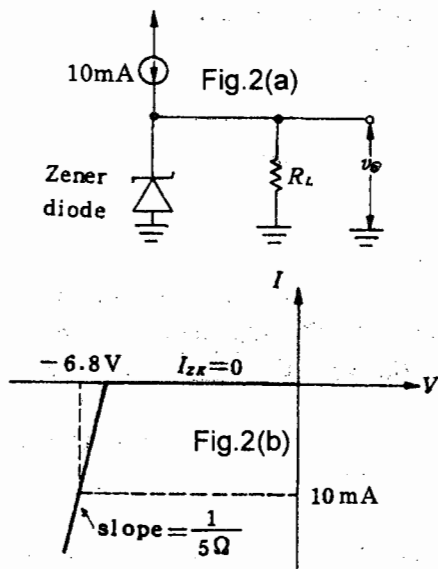

Fig. 1

2. A shunt voltage regulator consists of a Zener diode supplied by a constant current of 10 mA. At this operating current the Zener resistance is 5Ω and the Zener voltage is 6.8 V. The circuit and diode I-V characteristics are shown in Fig.2(a) and Fig.2(b), respectively. If the regulator is loaded by a resistor of $2k\Omega$, the output voltage decreased by_____mV.(10%)

Fig.2(a)

Fig.2(b)

2. In the circuit of Fig. 3, the NMOS transistor has $|V_t|$=0.9V and V_A=50 V and operates with V_D=2V. Find the v_o/v_i = _____V/V。(10%)

4. In the circuit of Fig. 4, v_{sig} is a small sine-wave signal with zero average. The transistor has β=100. (a) When the R_E= _____Ω, the transistor has a dc emitter current of about I_E=0.5 mA(5%) (b) When the R_C= _____Ω, the transistor has a dc collector voltage of about V_C=5 V(5%) (c) When the R_L= 10 kΩ and r_o= 200 kΩ, the overall voltage gain Av= v_o/v_{sig} = _____V/V. (5%)
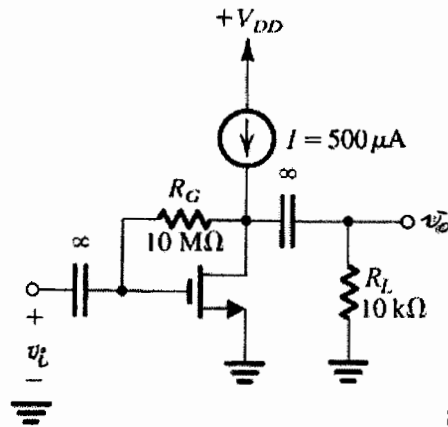
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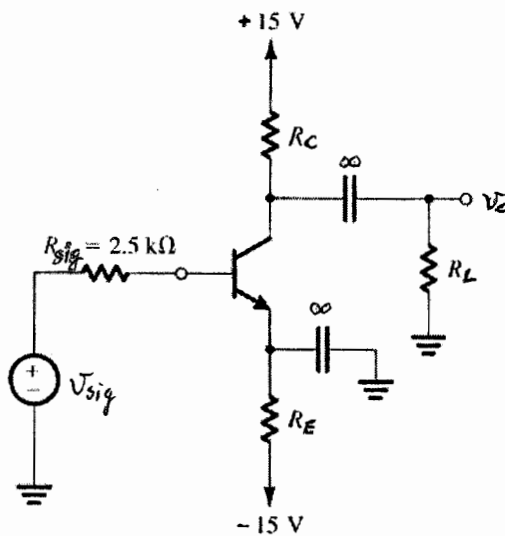

Fig.3

Fig.4

5. A feedback circuit is shown in Fig. 5, find (a) I_{out}/I_{in} and (b) R_{out}. Assume the transistors to have $\beta=100$ and $V_A=75$ V. (20%)
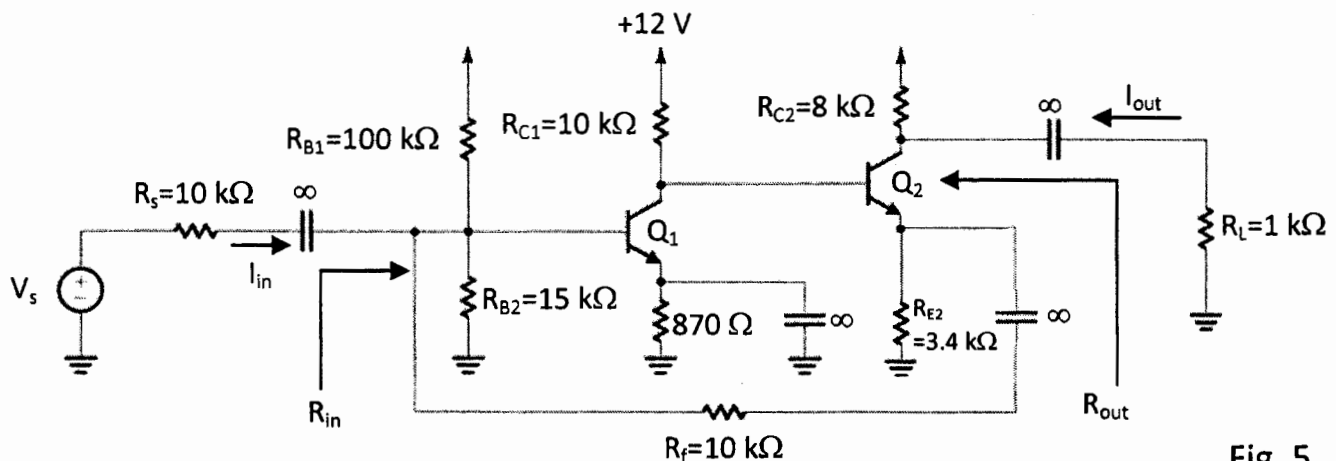

Fig. 5

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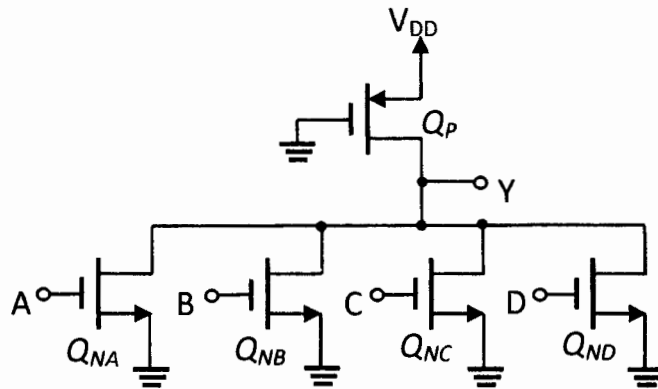6. In Fig. 6, find the digital logic relationship between Y and A, B, C, and D. (15%)

Fig. 6

7. For the circuit in Fig. 7 in which the transistors have $V_{BE}=0.7$ V and $\beta=100$, find g_{meq}, v_o/v_i, and R_{in}. (15%)
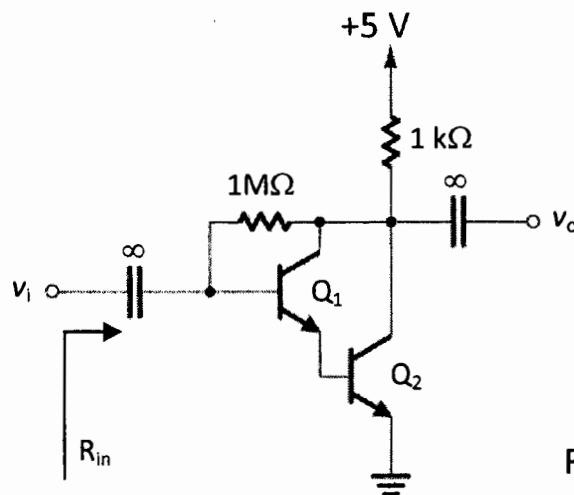

Fig. 7