編號： 45

國立成功大學 106 學年度碩士班招生考試試題

系　　所：光電科學與工程學系

考試科目：電子學

考試日期：0214，節次：1

※ 考生請注意：本試題不可使用計算機。　請於答案卷(卡)作答，於本試題紙上作答者，不予計分。

1. An pn junction operating in the forward-bias region with a current of 1 mA is found to have a diffusion capacitance of 10 pF (at temperature of 300K). What diffusion capacitance do you expect this junction to have at $I = 0.1$ mA? (5%) What is the mean transit time for this junction? (5%)

2. Figure 1 shows a circuit that performs the high-pass, single-time-constant function. Such a circuit is known as a first-order high-pass active filter. Derive the transfer function and show that the high-frequency gain is $(-R_2/R_1)$ and the 3-dB frequency $\omega_0 = 1/(CR_1)$. Design the circuit to obtain a high-frequency input resistance of 10 kΩ, a high-frequency gain of 40 dB, and a 3-dB frequency of 1 kHz. At what frequency does the magnitude of the transfer reduce to unity? (10%)

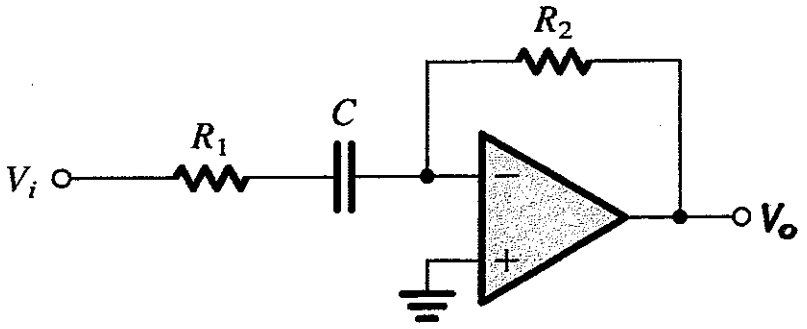

Figure 1.

3. In the circuit shown in Figure 2, I is a dc current and υ_i is a sinusoidal signal with small amplitude (less than 10 meV) and a frequency of 100 kHz. Representing the diode by its small-signal resistance r_d, which is a function of I, sketch the circuit for determining the sinusoidal output voltage V_0, and find the phase shift between V_i and V_0. Find the value of I that will provide a phase shift of -45°. Assume n=1. (10%)

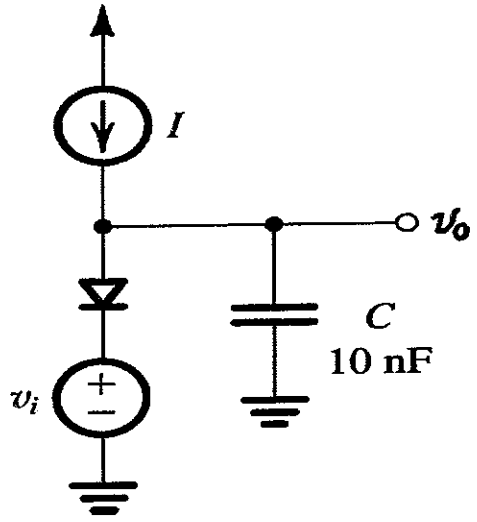

Figure 2.

4. The transistor in Figure 3(a) is biased with a constant current source $I = 1$ mA and has $\beta = 100$ and $V_A = 100$ V.

(a) Find transconductance (g_m), small-signal input resistance between base and emitter (r_π), and output resistance (r_0) (10%).

(b) If terminal Z is connected to ground, X to a signal source υ_{sig} with a source resistance $R_{sig} = 2$ kΩ, and Y to an 8-kΩ load resistance, use the hybrid-π small-signal model of Figure 3(b), to draw the small-signal equivalent circuit of the amplifier. (Note that the current source I should be replaced with an open circuit.) Calculate the overall voltage gain $\upsilon_y / \upsilon_{sig}$. If r_o is neglected, what is the error in estimating the gain magnitude? (10%)

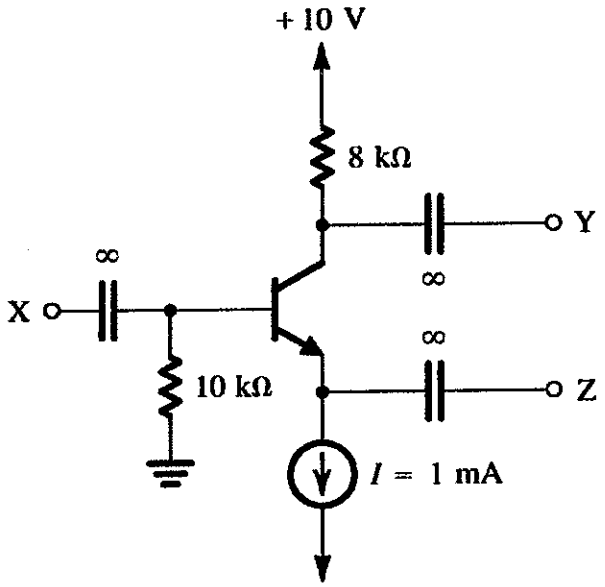

Figure 3(a)

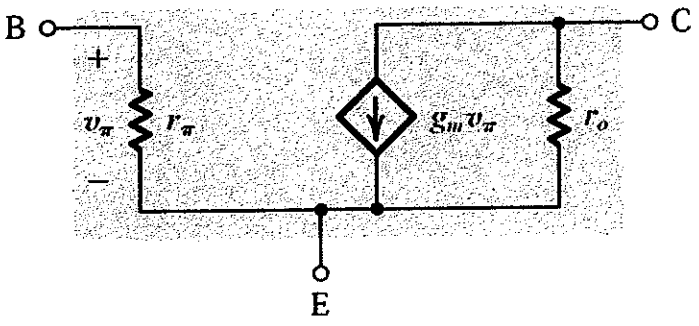

Figure 3(b)

5. Please using four NMOS transistors to plot the cascode MOS current mirror circuit. (10%)
6. For the devices in the circuits of Figure 4, $|V_t| = 1$ V, $\lambda = 0$, $\mu_n C_{ox} = 50\ \mu A/V^2$, L= 1 μm, and W= 10 μm. Find (a) V_2 (5%) and (b) I_2 (5%). When Q_3 and Q_4 are made to have W = 100 μm, how are the values of (c) V_2 (5%) and (d) I_2? (5%)

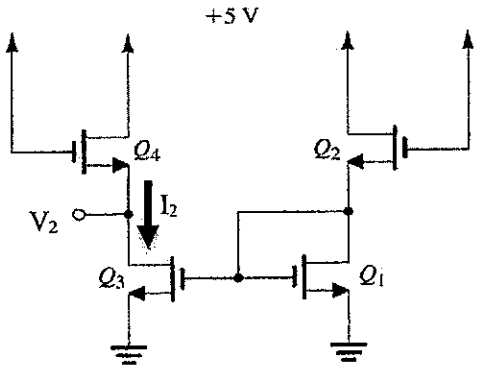

Figure 4

7. The differential amplifier in Figure 5 uses transistors with β = 100. Evaluate the following: (a) The input differential resistance R_{id}. (5%) (b) The overall differential voltage gain $\upsilon_{od}/\upsilon_{sig}$ (neglect the effect of r_o). (5%) (c) The worst-case common-mode gain if the two collector resistances are accurate to within ±1%. (5%) (d) The input common-mode resistance (assuming that the Early voltage V_A = 100 V). (5%)

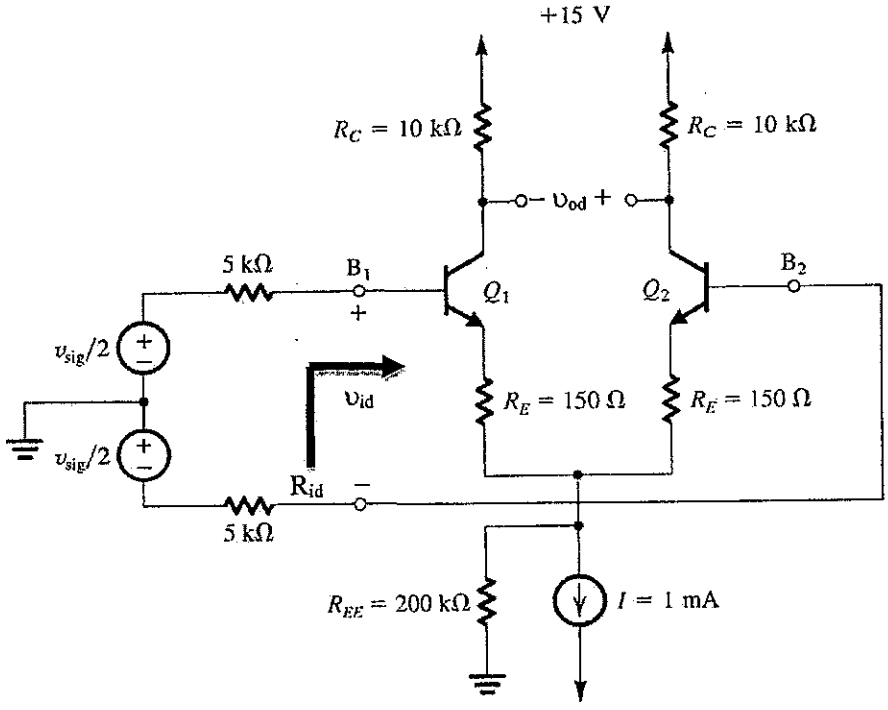

Figure 5