國立成功大學

110學年度碩士班招生考試試題

編　號：41

系　所：光電科學與工程學系

科　目：電子學

日　期：0203

節　次：第 1 節

備　註：不可使用計算機

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※ 考生請注意：本試題不可使用計算機。　請於答案卷(卡)作答，於本試題紙上作答者，不予計分。

1. The circuit in Fig. 1 implements a complementary-output rectifier. Assume a 0.7 V drop across each conducting diode. If the magnitude of the average of each output is to be 12 V, (a) find the required amplitude of the sine wave across the entire secondary winding. (10%) (b) What is the PIV of each diode? (10%)

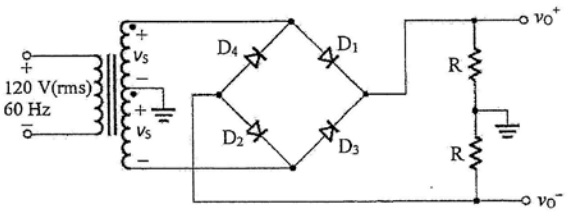

Fig. 1

2. For the emitter-follower circuit in Fig. 2, the β of BJT is 200. Find (a) base voltage V_B (5%), (b) input resistance R_{in} (5%), and (c) the voltage gain v_o/v_{sig} (5%).

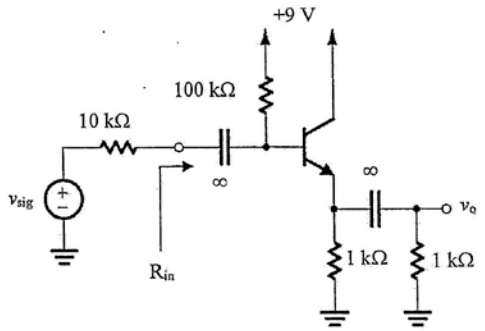

Fig. 2

3. The PMOS transistor in the common-source (CS) amplifier of Fig. 3 has V_{tp}= –0.7 V and a very large $|V_A|$.

(a) Select a value for R_S to bias the transistor at I_D= 0.3 mA and $|V_{OV}|$= 0.3 V. Assume v_{sig} to have a zero dc component. (5%)

(b) Select a value for R_D that results in voltage gain G_v= –10 V/V. (5%)

(c) Find the largest sinusoid $\hat{v}_{sig}$ that the amplifier can handle while remaining in the saturation region. What is the corresponding signal at the output? (5%)

(d) If to obtain reasonably linear operation, $\hat{v}_{sig}$ is limited to 50 mV, what value can R_D be increased to while

maintaining saturation-region operation? (5%) What is the new value of G_v? (5%)

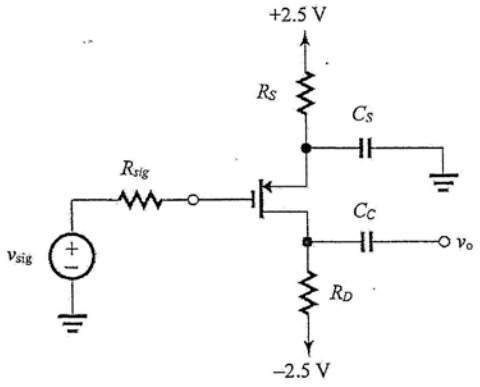

Fig. 3

4. A differential amplifier shows in Fig. 4. Please find the differential gain, the differential input resistance, the common mode gain, common mode rejection ratio, and common mode input resistance. For these transistors, β=100 and V_A= 100V. (20%)

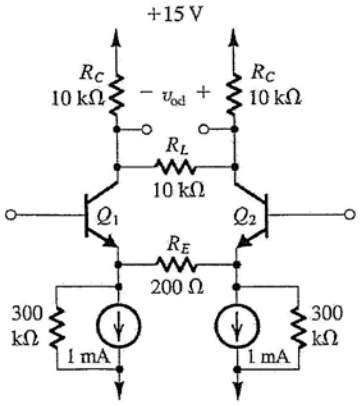

Fig. 4

5. Please find the low-frequency gain, the frequency of the pole, and the frequency of zero of the circuit showing in Fig. 5. The DC-bias current is 100μA. For Q_1, $\mu_n C_{ox}$ = 90 μA/V^2, V_A=12.8 V, W/L = 100 μm/1.6μm, C_{gs} = 0.2 pF, C_{gd} = 0.015 pF, and C_{db} = 20 fF. For Q_2, C_{gd} = 0.015 pF, C_{db} = 36 fF, and $|V_A|$ = 19.2 V. Assume that the resistance of the input signal generator is negligibly small. And for simplicity, assume that the signal voltage at the gate of Q_2 is zero. (20%)

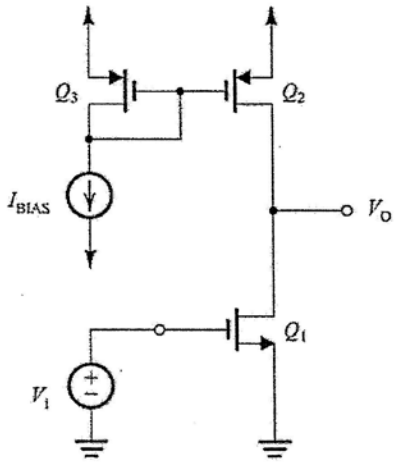

Fig. 5