Complete questions : 30%

1. Holes are being steadily injected into a region of n-type silicon. In the steady state, the excess-hole concentration profile shown in fig.1 is established in the n-type region. If $N_D=10^{16}cm^{-3}$, $n_i=1.5x10^{10}cm^{-3}$ and W=5μm, what is the density of current J_x (1) that will flow in the x direction.

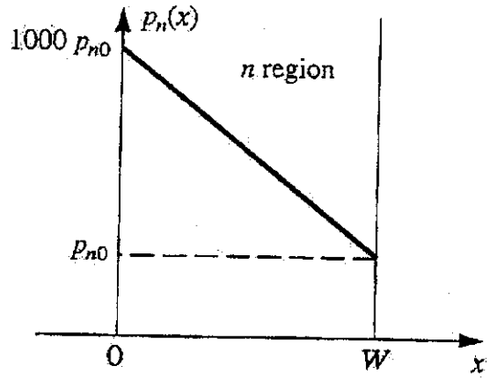

Fig. 1

2. If for a particular junction, $N_A=10^{16}cm^{-3}$, $N_D=10^{15}cm^{-3}$, find the junction built in voltage V_{bi} (2). Assume $n_i=10^{10}cm^{-3}$. Also, find the width of depletion region (W_{dep}) (3) and its extent in n (4) region when the junction is reverse biased with V_R=5V. Assume the junction area is $400\mu m^2$. Also, calculate C_j (5).
3. Consider a CMOS process for which L_{min}=0.8μm, t_{ox}=15nm, $\mu_n=550cm^2/V.s$, and V_t=0.7V. $\varepsilon_{ox}=3.45x10^{-11}F/m$
   (a) find C_{ox} (6) and k_n' (7).
   (b) For an NMOS transistor with W/L=16μm/0.8μm, calculate the values of V_{OV} (8), V_{GS} (9), and V_{DSmin} (10) needed to operate the transistor in the saturation region with a dc current I_D=100μA.
   (c) For the device in (b), find the value of V_{OV} (11) and V_{GS} (12) required to cause the device to operate as a 1000Ω resistor for very small v_{DS}
4. For the Darlington voltage follower in Fig. 2, find the R_{in} (13), R_{out} (14) and V_o/V_{sig} (15) for the case I_{E2}=5mA, $\beta_1=\beta_2=100$, R_E=1KΩ, and R_{sig}=100KΩ.

（背面仍有題目，請繼續作答）

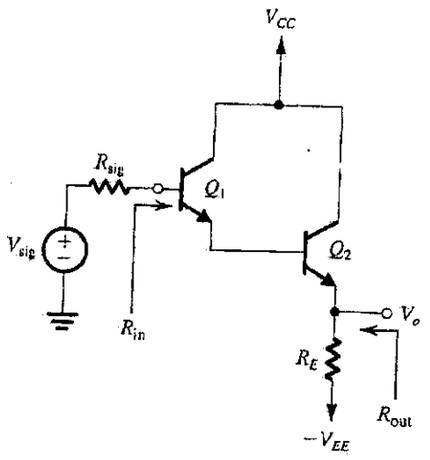

Fig. 2

Calculations : 70%

1. Find the differential voltage gain of the modified version difference amplifier of Fig. 3. (10%)

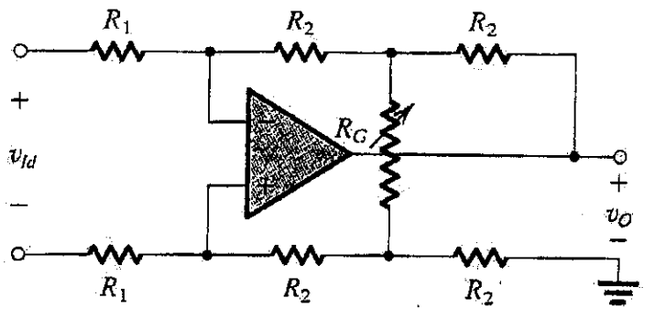

Fig. 3

2. Sketch and clearly label the transfer characteristic of the circuit in Fig.4 for -20V<v_I<+20V. Assume that the diodes can be presented by a piecewise-linear model with V_{DO}=0.65V and r_D=20Ω. Assuming that the specified Zener voltage (8.2V) is measured at current of 10mA and r_Z = 20Ω, represent the Zener by a piecewise-linear model. (10%)

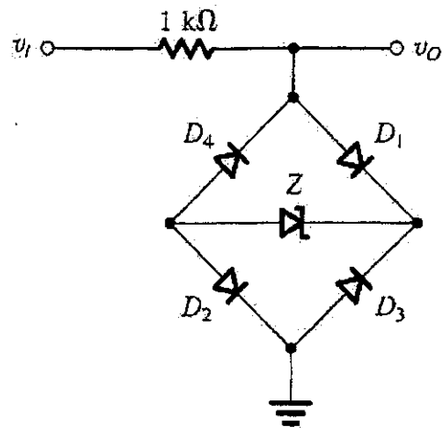

Fig. 4

3. Consider the circuit shown in Fig.5. For each transistor β=100 and each diode V_D = 0.7V, find the voltage V_{B1}, V_{E1}, V_{C1}, V_{B2}, V_{E2} and V_{C2}. (15%)

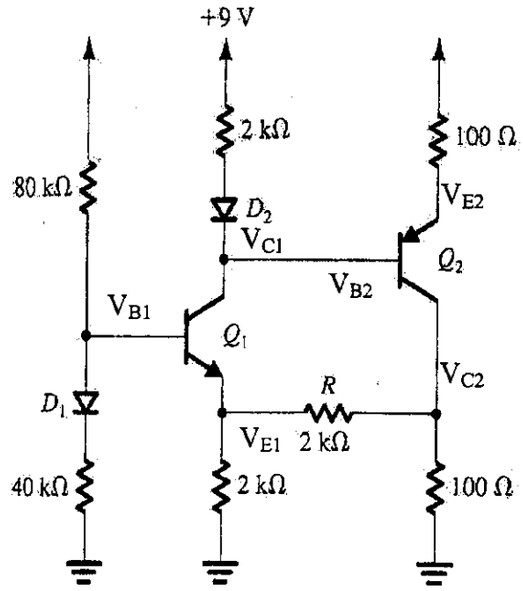

Fig. 5

4. Consider the differential amplifier shown in Fig. 6. Find the differential gain, the differential input resistance, the common mode gain and the common mode input resistance. For these transistors, β=100 and V_A=100V. (15%)

（背面仍有題目，請繼續作答）

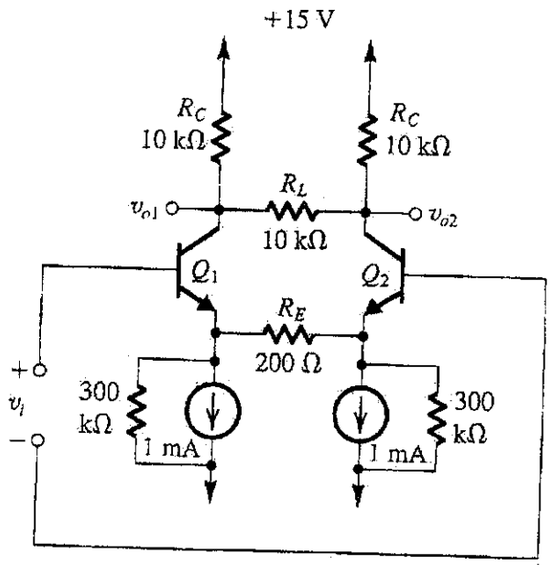

Fig. 6

5. The circuits shown in Fig. 7 employ negative feedback. Assume that each transistor is sized and biased so that g_m=1mA/V and r_0=100kΩ. Otherwise ignore all dc biasing detail and concentrate on small signal operation resulting in response to the input signal v_{sig}. for R_L=10kΩ, R_1=500KΩ, and R_2=1MΩ, find the overall voltage gain v_o/v_{sig} and the input resistance R_{in} for each circuit. Neglect the body effect. (20%)

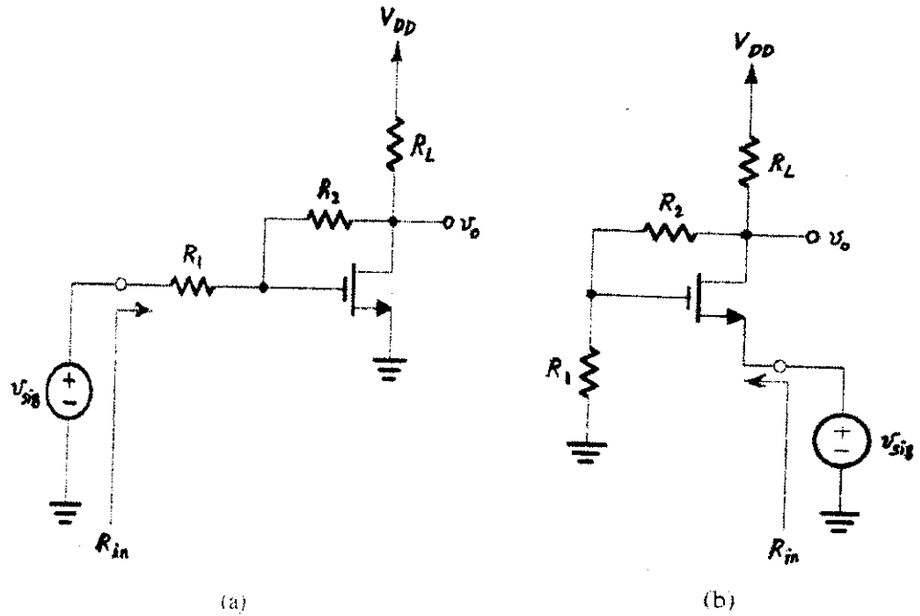

Fig. 7