編號：52　系所：光電科學與工程研究所　　科目：電子學

本試題是否可以使用計算機：☑可使用，☐不可使用　（請命題老師勾選）

1. If the forward transit-time τ_F must equal 7.5ps for a particular communications IC to get the maximum frequency response of Si BJT. The parameters of the device: Si dielectric constantan ε_{Si} = $11.7\times8.85\times10^{-14}$ F/cm, q = 1.6×10^{-19} coul., $n_i^2=2\times10^{20}cm^{-3}$, kT/q=25mV, V_{BE}=0.7V, ln2=0.693, ln5=1.609. (20%)
   (a) What is the required effective (neutral) base width W (in unit of nm)? Assuming that the electron diffusivity in the base is $D_{nB}=10cm^2/s$.
   (b) Assuming all pn junctions are abrupt. If the collector and base doping concentration are $N_{dC}=2\times10^{16}cm^{-3}$ and $N_{dB}=10^{17}cm^{-3}$ and the collector-emitter bias is V_{CE}=3V for part (a), find the distance W', which is defined as the distance between the edge of the emitter-base depletion region at the base side and the location of the base/collector junction.
2. A MOS amplifier was shown as Fig.1. Please find the Rin, Rout, and voltage gain. The current source is for DC bias only. Q1 and Q2 have small signal parameters as follows: the transconductances are g_{m1} for Q1 and g_{m2} for Q2, respectively. (20%)

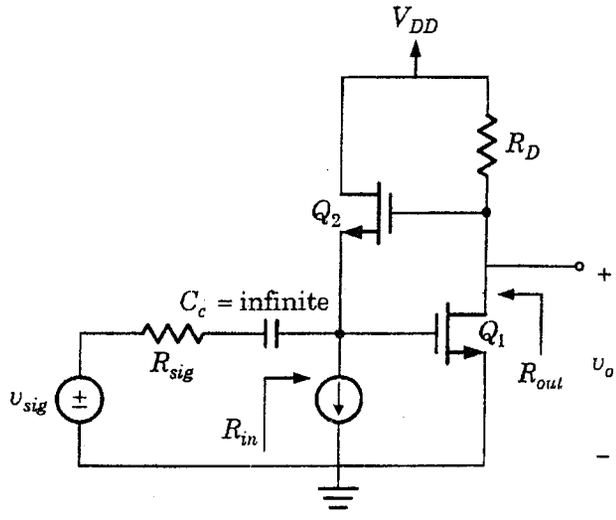

Fig.1

3. Assume the resistance of the input signal generator is negligibly small; the signal voltage at the gate of Q2 is zero. Analyze the high frequency response of the CMOS amplifier as shown in Fig. 2. The DC bias current is 100μA. For Q1, $\mu_nC_{ox}=90\mu A/V^2$, V_A=12.8V, W/L=100μm/1.6μm, and C_{gs}=0.2pF, C_{gd}=0.015pF and C_{db}=20fF. For Q2 and Q3, $\mu_nC_{ox}=30\mu A/V^2$, $|V_A|$=19.2V, C_{gd}=0.015pF and C_{db}=36fF. There is 0.3pF stray capacitance between the common drain connection and ground. (20%)
   (1) gm for Q1 is :
   (A) 0.106mA/V　(B) 0.053mA/V　(C) 1.06mA/V　(D)0.212mA/V
   (2) The output resistance of the amplifier is

（背面仍有題目，請繼續作答）

(A) 128KΩ (B)192kΩ (C) 320KΩ (D)76.8KΩ

(3) The low frequency voltage gain Av:

(A) -203V/V (B) -81.4V/V (C) -106V/V (D) -135V/V

(4) The frequency of the unity gain is:

(A) 11.25GHz (B) 4.75GHz (C) 2.38GHz (D) 5.65GHz

(5) The frequency of the pole (3dB) is:

(A) 24.1MHz (B) 2.41MHz (C) 550kHz (D) 5.37MHz

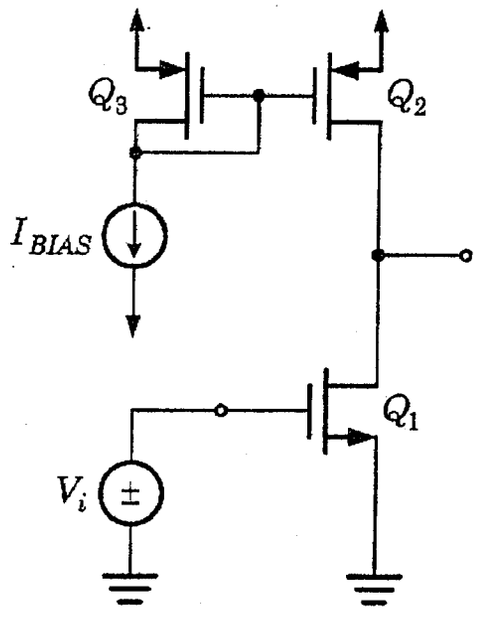

Fig.2

4. For the TTL gate shown in Fig.3, if the inputs are obtained from the outputs of similar gates and $h_{FE}(min)=20$, $h_{FEI} = 0.5$, $V_{BE(act)}=0.7V$, $V_{BE(sat)}=0.8V$ (20%)

(a) When all inputs are high, find the state of each transistor and all currents and voltages of the circuit.

(b) Repeat (a) if at least one input is low.

(c) Calculate the maximum fan-out for proper operation.

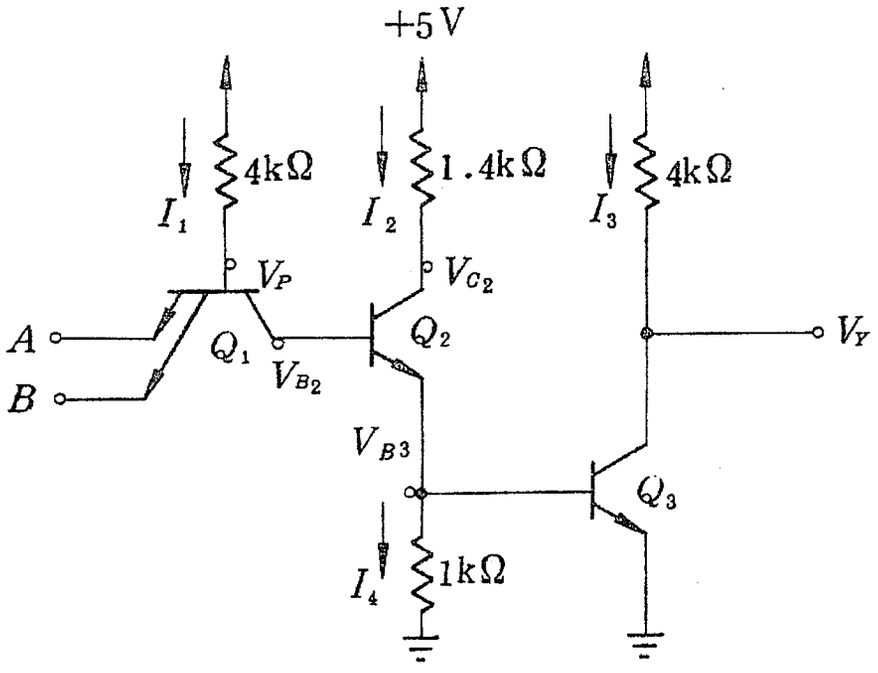

Fig.3

5. Fig. 4 shows the corresponding layout of the CMOS circuit. (20%)
   (a) Draw the circuit diagram of the Fig.4.
   (b) Assume V_{DD}=5V and electron and hole mobility μ_n= 600 cm^2/Vsec, μ_p=250 cm^2/Vsec. If the channel lengths and widths of the two devices are as shown in the figure, determine the inverter switching threshold (V_{th}), V_A and V_B.
   (c) What is the voltage gain of this circuit at V_{OUT}=V_{IN}?
   (d) Explain why $(W/L)_p \neq (W/L)_n$?

（背面仍有題目,請繼續作答）

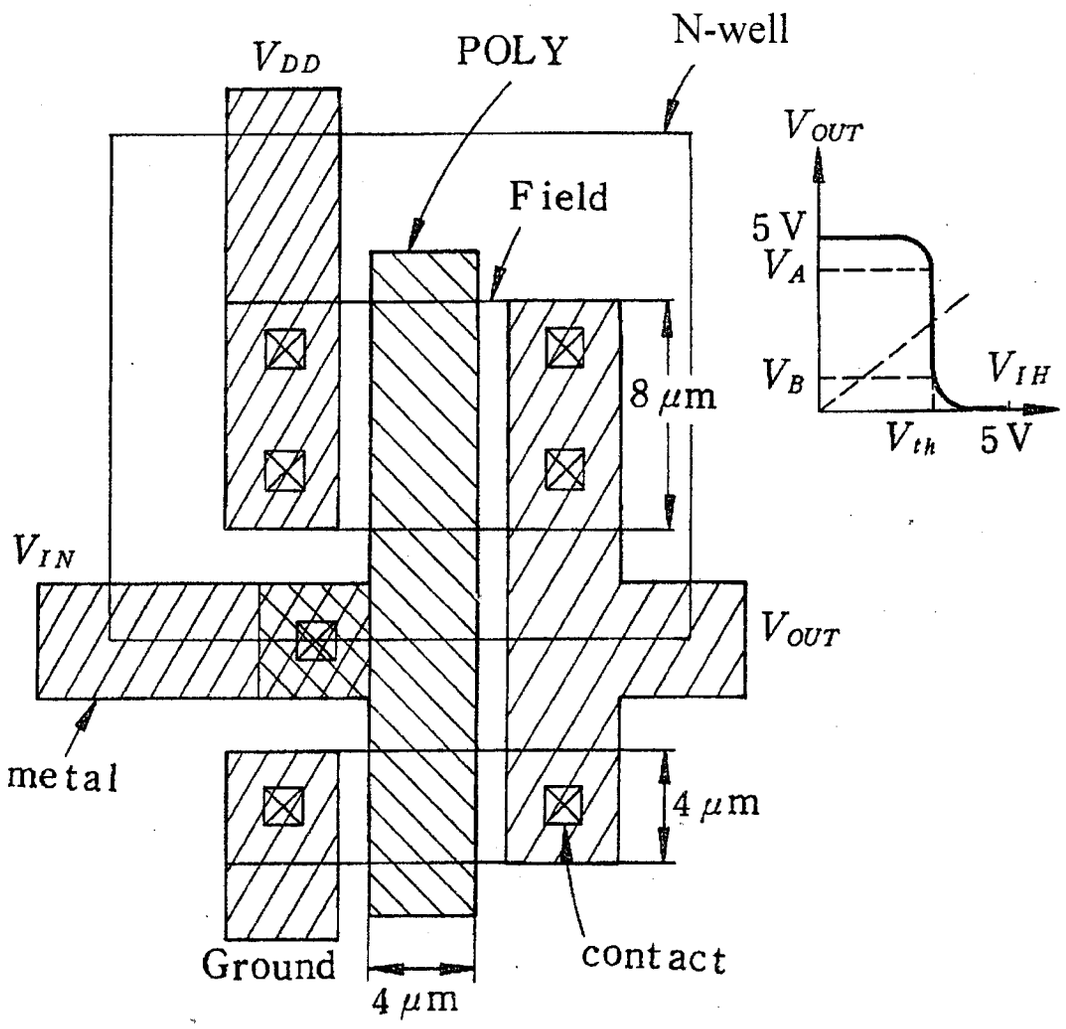
V_{DD}
POLY
N-well
Field
8 μm
V_{IN}
V_{OUT}
metal
4 μm
Ground
contact
4 μm
V_{OUT}
5 V
V_A
V_B
V_{IH}
V_{th}
5 V

Fig. 4