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1. For the ampilifer in the Fig. 1, let the parameters of transistors M1, M2 and Q1 $\mu_n C_{ox}=200\mu A/V^2$, $V_t=1V$, $(W/L)_{M1}=10$, $(W/L)_{M2}=20$ and β (Q1)=499. Please find
(a) Output DC voltage v_o (10%)
(b) Small signal voltage gain v_o/v_i. (10%)

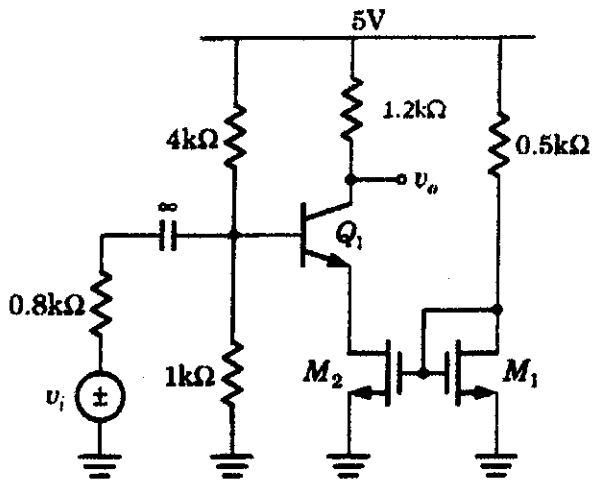

Fig. 1

2. The differential amplifier circuit of Fig. 2 utilizes a resistor connected to the negative power supply to establish the bias current I. where Q_1 and Q_2 α~1
(a) For $v_{B1}=v_{id}/2$ and $v_{B2}=-v_{id}/2$ where v_{id} is a small signal with zero average, find the magnitude of the differential gain, $|v_o/v_{id}|$ (5%)
(b) For $v_{B1}=v_{B2}=v_{icm}$, find the magnitude of the common-mode gain, $|v_o/v_{icm}|$. (5%)
(c) Find the CMRR. (5%)

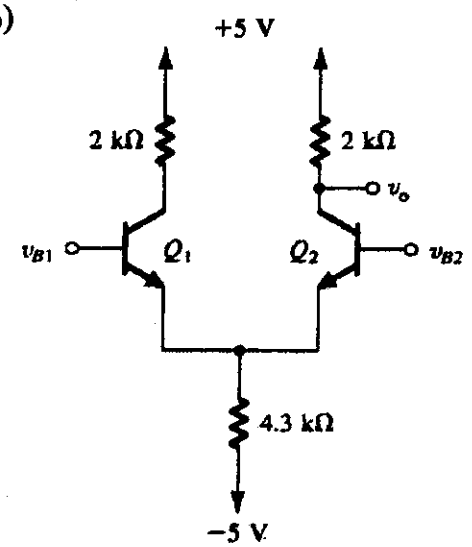

Fig. 2

(背面仍有題目，請繼續作答)

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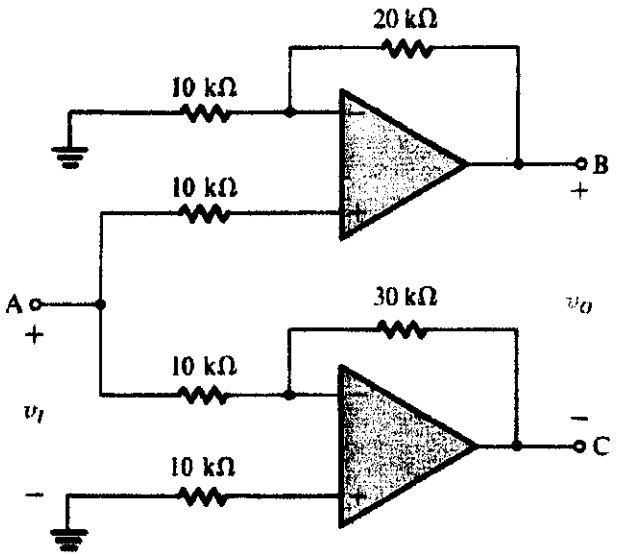
3. The circuit shown in fig. 3 is intended to supply a voltage to floating loads while making greatest possible use of the available power supply.
(a) Assuming ideal OP amps, sketch the voltage waveforms at nodes B and C for a 1-V peak-to-peak sine wave applied at node A. Also sketch the v_o. (5%)
(b) What is the voltage gain v_o/v_i. (5%)
(c) Assuming that the OP amps operate from ±15-V power supplies and that their output saturates at ±14V. What is the largest sine wave output that can be accommodated? Specify both its peak to peak and rms values. (5%)

Fig. 3



4. For the circuits in Fig. 4, $\mu_n C_{ox}$ =2.5 $\mu_p C_{ox}$ = 20 μA/V^2, $|V_t|$= 1V, λ =0, γ =0, L =10 μm, and W = 30 μm, unless otherwise specified. Find the labeled currents and voltages. (15%)

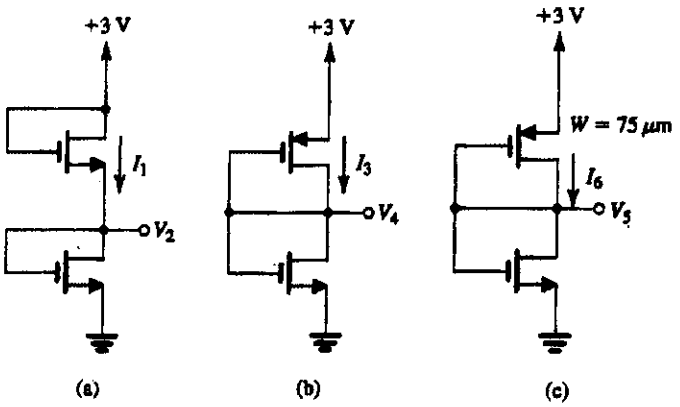


Fig. 4

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5. For a digital logic inverter fabricated in a 0.8-μm CMOS technology for which k_n' = 120 μA/V^2, k_p' = 60 μA/V^2, $V_{tn} = |V_{tp}|$ = 0.7 V, V_{DD} = 3 V, $L_n = L_p$ = 0.8 μm, W_n = 1.2 μm, and W_p = 2.4 μm, find:

(a) the output resistance for $v_O = V_{OL}$, and for $v_O = V_{OH}$ (5%)

(b) the maximum current that the inverter can sink or source while the output remains within 0.1 V of ground or V_{DD}, respectively (5%)

(c) V_{IH}, V_{IL}, and noise margins NM_H, NM_L (5%)

(d) the peak current drawn from the 3-V supply during switching (5%)

6. For the transistor shown in Fig. 5, assume α=1 and v_{BE} =0.5 V at the edge of conduction. What are the values of V_E and V_D for V_B = 0V? For what value of V_B does the transistor cut off? Saturate? In each case, what values of V_E and V_C result? (15%)

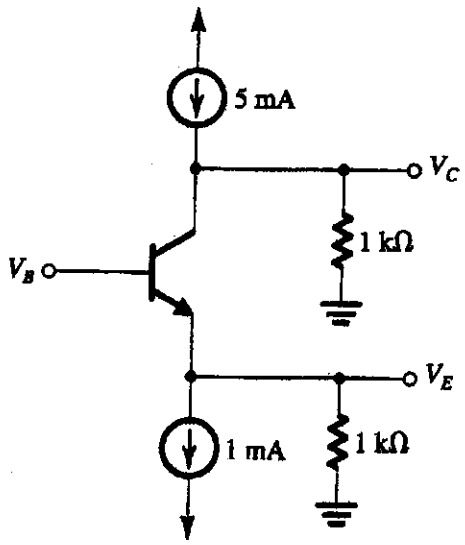

Fig. 5