

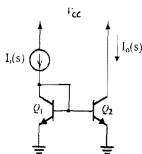
系所組別 光電科學與工程研究所乙組

考試科目 電子學

考試日期 · 0306 期次 1

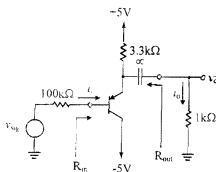
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1. For the current mirror in the right figure derive an expression for the current transfer function  $I_o(s)/I_i(s)$  taking into account the BJT internal capacitances and neglecting  $r_x$  and  $r_o$ . Assume the BJTs to be identical. Observe that a signal ground appears at the collector of  $Q_2$ . If the mirror is biased at 1mA and the BJTs at this operating point are characterized by  $f_T=400\text{MHz}$ ,  $C_\mu=2\text{pF}$ , and  $\beta_0=\infty$ , find

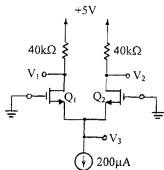


- (a) the frequencies of the pole ( $f_p$ ) of the transfer function.  $f_p = \underline{\hspace{2cm}}$  (7%)  
 (b) the frequencies of the zero ( $f_z$ ) of the transfer function.  $f_z = \underline{\hspace{2cm}}$  (6%)

2. For the emitter follower in the right figure, the signal source is directly coupled to the transistor base. If the dc component of  $v_{sig}$  is zero. (a) find the dc emitter current (5%). Assume  $\beta=100$ . Neglecting  $r_o$ . (b) find  $R_{in}$  (5%), (c) the voltage gain  $v_o/v_{sig}$  (5%). (d) the current gain  $i_o/i_i$  (5%). and (e) the output resistance  $R_{out}$  (5%)



3. In the below figure, transistors  $Q_1$  and  $Q_2$  have  $V_{T1}=1\text{V}$ , and the process transconductance parameter  $k_n'=100\mu\text{A}/\text{V}^2$ . Assuming  $\lambda=0$ , find  $V_1$ ,  $V_2$ , and  $V_3$  for  $(W/L)_1=1.5(W/L)_2$ . (12%)



(背面仍有題目,請繼續作答)

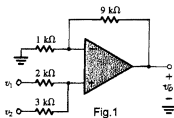
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- 4.(a) Use the superposition principle to find the output voltage of the circuit shown in Fig.1.(b) If in the circuit of Fig.1 the 1-k $\Omega$  resistor is disconnected from ground and connected to a third signal source  $v_3$ , use superposition to determine  $v_0$  in term of  $v_1$ ,  $v_2$  and  $v_3$ .(10%)



5. Consider a Si n-channel MOSFET with channel width  $W=15 \mu\text{m}$ , length  $L=2 \mu\text{m}$ , gate oxide thickness  $t_{ox}=0.5 \mu\text{m}$ , dielectric constant  $\epsilon_{ox}=3.9$ . Assume that the drain current in the saturation region for  $V_{DS}=0.10\text{V}$  is  $I_D=3.5\text{mA}$  at  $V_{GS}=1.5\text{V}$  and  $I_D=75 \mu\text{A}$   $V_{GS}=2.5\text{V}$ . (a) Please find the inversion carrier mobility ( $\mu_n$ ) in channel and the threshold voltage ( $V_T$ ). (b) please comment the determined  $\mu_n$  compared with the bulk mobility.(10%)
6. As shown in Figure 2, if the five light output power-current (L-I) curves correspond to a GaAs LED operated at different pulsed injection currents, i.e., different duty cycles, which is defined in the inset of Figure 2. Please identify which of the following item(s) is(are) true.(A) duty 1 > duty 2 (B) duty 3 > duty 4 (C) duty 2 > duty 5 (D) duty 3 > duty 2 (E) duty 5 > duty 4 (2%)

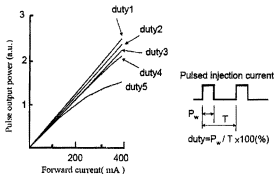
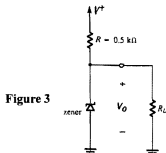


Figure 2

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7. Under thermal equilibrium, which of the following approach(es) can create a built-in electric field in a semiconductor?(A)p-n junction(B) spatial variation of doping concentration(C)n-type GaAs(D)intrinsic Si.(2%)
8. The zener diode in the circuit of Figure 3 is specified to have  $V_Z=6.8V$  at  $I_Z=5$  mA,  $r_z=20\ \Omega$  and  $I_{zk}=0.2$  mA. The power supply voltage  $V^+=10V$ .  
(A)  $V_o = 6.83$  V with no load (B)  $I_L=13.6$  mA when  $R_L=0.5K\Omega$ (C)  $V_o = 5$  V when  $R_L=0.5K\Omega$  (D)  $I_Z = 6.35$  mA with no load (6%)



9. The threshold voltage will increase for a n-channel MOS FET when (A)increase the reverse bias of substrate increase (B) decrease the doping concentration of substrate (C)increase the thickness of gate oxide (D) increase the gate length. (3%)
10. Which of the following statement(s) is(are) true(A)The BJT transconductance increases exponentially with respect to  $V_{BE}$ .(B)The MOS FET's transconductance increases linearly with respect to  $V_{GS}$ .(C)A PMOS FET has four terminals(D)Compared with MOS FET, BJT device has higher input impedance. (3%)

(背面仍有題目,請繼續作答)

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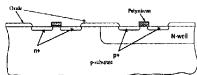
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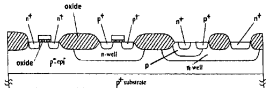
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11. Please identify the following schematic device.

(a) \_\_\_\_\_ (2%)



(b) \_\_\_\_\_ (2%)



12. Determine the output voltage  $V_o$  in the following circuit when (a)  $V_1=V_2=5V$  (5%)(b)  $V_1= 5V, V_2=0$ . Assume that the  $D_1$  is identical to  $D_2$  with  $r_D=30 \Omega$ ,  $V_{D0}=0.6V$ (5%)

